

876534321

MSB = 507
ON = 0

FUNCTION GENERATOR NEST

TERMINATION

1

COMBINER

3

FG1 B0

5

FG2 B4

7

FG3 B8

9

FG4 BC

11

4	A3	3	A2	2	A1	1	A0
2X3	A7	1X2	A6	6	A5	5	A4

12

13

FG5 C0

15

FG6 C4

17

SPARE

19

FG SEL	INTENS	9B	BLUE	9A	GREEN	99	RED	98
--------	--------	----	------	----	-------	----	-----	----

21

FG SEL	DEPTH	97	VERT	96	WIDTH	95	HORIZ	94
--------	-------	----	------	----	-------	----	-------	----

23

FG SEL	SPARE	93	SPARE	92	HBLW	91	HBLST	90
--------	-------	----	-------	----	------	----	-------	----

25

Termination or Spare

25

MDAC
CIC-1-1
MDAC
CIC-1-1

RPU NEST 3

FUNCTION GENERATOR + COMBINER

11 FG 4				9 FG 3				7 FG 2				5 FG 1				3 COMBINER				Select			
1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1			62
2	+5	GND	63		+5	GND			+5	GND			+5	GND			+5	GND		2			63
3	RPU STROBE	-5	64																	3			64
4	RPU WHITE	SYNCH SRT	65																	4			65
5	HSYNCH	FSYNCH	66	5			66	5			66	5			66	5			66	5			66
6	SSYNCH	VSYNCH	67																	6			67
7	CON 1	SYNCH SRT	68																	7			68
8	CON 0	RPU TO SET	69																	8			69
9	BUSSE R	RPUA 0	70																	9			70
10	RPU 0 0	RPUA 1	71	10			71	10			71	10			71	10			71	10			71
11	RPU 0 1	RPUA 2	72																	11			72
12	RPU 0 2	RPUA 3	73																	12			73
13	RPU 0 3	RPUA 4	74																	13			74
14	RPU 0 4	RPUA 5	75																	14			75
15	RPU 0 5	RPUA 6	76	15			76	15			76	15			76	15			76	15			76
16	RPU 0 6	RPUA 7	77																	16			77
17	RPU 0 7	RPUA 8	78																	17			78
18	RPU 0 8	RPUA 9	79																	18			79
19	RPU 0 9	RPUA 10	80																	19			80
20	RPU 0 10	RPUA 11	81	20			81	20			81	20			81	20			81	20			81
21	RPU 0 11	RPUA 12	82																	21			82
22	RPU 0 12	RPUA 13	83																	22			83
23	RPU 0 13	RPUA 14	84																	23			84
24	RPU 0 14	RPUA 15	85																	24			85
25	RPU 0 15	VBLANK	86	25			86	25			86	25			86	25			86	25			86
26	RPU 0 16	MCCLK	87																	26			87
27	SPARE 1	SPARE 2	88																	27			88
28			89																	28			89
29	FG 407				FG 307				D7							FG 107				29			90
30	FG 406		10		FG 306		91	30			FG 206		91	30		FG 106		91	30				91
31	FG 405		11		FG 305			FG 205			FG 105			FG 205	FG 105					31			92
32	FG 404		12		FG 304			FG 204			FG 104			FG 204	FG 104					32			93
33	FG 403		13		FG 303			FG 203			FG 103			FG 203	FG 103					33			94
34	FG 402		14		FG 302			FG 202			FG 102			FG 202	FG 102					34			95
35	FG 401		15	35	FG 301		96	35			FG 201		96	35	FG 101		96	35		35			96
36	FG 400		16		FG 300			FG 200			FG 100			FG 200	FG 100					36			97
37	LDAC 4		17		LDAC 3			LDAC 2			LDAC 1			FG 200	LDAC 1	TWISTED PAIR ON ALL LDAC SIGNALS				37			98
38			18											38	LDAC 2					38			99
39			19												FG 207					39	FG 107		100
40			20				101	40			101	40			FG 307	FG 207		101	40		2A		101
41			21												FG 306	FG 206				41	1x2A		102
42			22												FG 305	FG 205				42	3A		103
43			23												FG 304	FG 204				43	2x3A		104
44			24												FG 303	FG 203				44	4A		105
45			25				106	45			106	45			FG 302	FG 202		106	45		5A		106
46			26												FG 301	FG 201				46	6A		107
47			27												FG 300	LDAC 2				47			108
48			28												48	LDAC 3				48			109
49			29																	49			110
50			30				111	50			111	50						111	50				111
51	V4OUT		31	51	V3OUT			V2OUT			V1OUT				Vcomb1					51			112
52			32												Vcomb2					52			113
53	+15		33		+15			+15			+15				+15					53			114
54			34																	54			115
55	-15		35		-15		116	55		-15	116	55		-15	116	55		-15	116	55			116
56			36																	56			117
57	GND I		37		GND I			GND I			GND I				GND I					57			118
58			38																	58			119
59			39																	59			120
60	+5	GND	40	60	+5	GND	121	60	+5	GND	121	60	+5	GND	121	60	+5	GND	121	60			121
61	+5	GND	41	61	+5	GND	122	61	+5	GND	122	61	+5	GND	122	61	+5	GND	122	61			122

— DENOTES SIGNALS BUSSED ACROSS BACKPLANE

RPU NEST 2

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
40	100 VERT BLKG START	BIN		10			
41	101 VERT BLKG WIDTH	BIN		10			
42	102 MISC 1 (SEC OV, EX3, SB, VIDEO SEL)			6			
43	103 OVERLAP (FRAME)			1			
100	400 CONTROL 1 (RATES, 3D)			3			
48	110 H POSITION CFG AMP	OFF	MD	12	+10	HF	CIC-1-1
49	111 V POSITION	↓	↓	↓	↓	↓	↓
4A	112 WIDTH	↓	↓	↓	↓	↓	↓
4B	113 DEPTH	↓	↓	↓	↓	↓	↓
50	120 WIDTH	OFF	D	12	+10	LF	CIC-1-2
51	121 D PAR	↓	↓	↓	↓	↓	↓
52	122 H PAR	↓	↓	↓	↓	↓	↓
53	123 L PAR	↓	↓	↓	↓	↓	↓
58	130 I PAR	OFF	MD	12	+10	HF	CIC-1-1
59	131 J PAR	↓	↓	↓	↓	↓	↓
5A	132 K PAR	↓	↓	↓	↓	↓	↓
5B	133 DEPTH	↓	D	↓	↓	↓	↓
60	140 A PAR	OFF	MD	12	+10	HF	CIC-1-1
61	141 B PAR	↓	↓	↓	↓	↓	↓
62	142 E PAR	↓	↓	↓	↓	↓	↓
63	143 F PAR	↓	↓	↓	↓	↓	↓
68	150 C PAR	OFF	MD	12	+10	HF	CIC-1-1
69	151 G PAR	↓	↓	↓	↓	↓	↓
6A	152 H BLKG START CFG	↓	↓	↓	↓	↓	↓
6B	153 H BLKG WIDTH CFG	↓	↓	↓	↓	↓	↓

RPU NEST 1

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
0	0 INTENSITY CFG AMP	OFF	MD	8	+10	HF	CIC-1-4
1	1 RED 1	↓	↓	↓	↓	↓	↓
2	2 GREEN 1	↓	↓	↓	↓	↓	↓
3	3 BLUE 1	↓	↓	↓	↓	↓	↓
8	10 IC 1 (AF-BE)	OFF	MD	12	+10	HF	CIC-1-1
9	11 IC 2 (BI-AJ)	↓	↓	↓	↓	↓	↓
A	12 IC 3 (JE-FI)	↓	↓	↓	↓	↓	↓
B	13 SPARE	↓	↓	↓	↓	↓	↓
10	20 INTENSITY	BIN	D	8	+10	LF	CIC-5
11	21 RED 1	↓	↓	↓	↓	↓	↓
12	22 GREEN 1	↓	↓	↓	↓	↓	↓
13	23 BLUE 1	↓	↓	↓	↓	↓	↓
14	24 RED 2	↓	↓	↓	↓	↓	↓
15	25 GREEN 2	↓	↓	↓	↓	↓	↓
16	26 BLUE 2	↓	↓	↓	↓	↓	↓
17	27 RED 3	↓	↓	↓	↓	↓	↓
18	30 GREEN 3	BIN	D	8	+10	LF	CIC-5
19	31 BLUE 3	↓	↓	↓	↓	↓	↓
1A	32 RED 4	↓	↓	↓	↓	↓	↓
1B	33 GREEN 4	↓	↓	↓	↓	↓	↓
1C	34 BLUE 4	↓	↓	↓	↓	↓	↓
1D	35 RED 5	↓	↓	↓	↓	↓	↓
1E	36 GREEN 5	↓	↓	↓	↓	↓	↓
1F	37 BLUE 5	↓	↓	↓	↓	↓	↓

RPU NEST 1

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
20	40 AUX 1	OFF	D	12	± 10	LF	CIC-1-2
21	41 AUX 2	↓	↓	↓	↓	↓	↓
22	42 AUX 3	↓	↓	↓	↓	↓	↓
23	43 AUX 4	↓	↓	↓	↓	↓	↓
28	50 AUX 5	OFF	D	12	± 10	LF	CIC-1-2
29	51 AUX 6	↓	↓	↓	↓	↓	↓
2A	52 SPARE	↓	↓	↓	↓	↓	↓
2B	53 SPARE	↓	↓	↓	↓	↓	↓

30-37 60-67 } SPARES
 38-3F 70-77 }

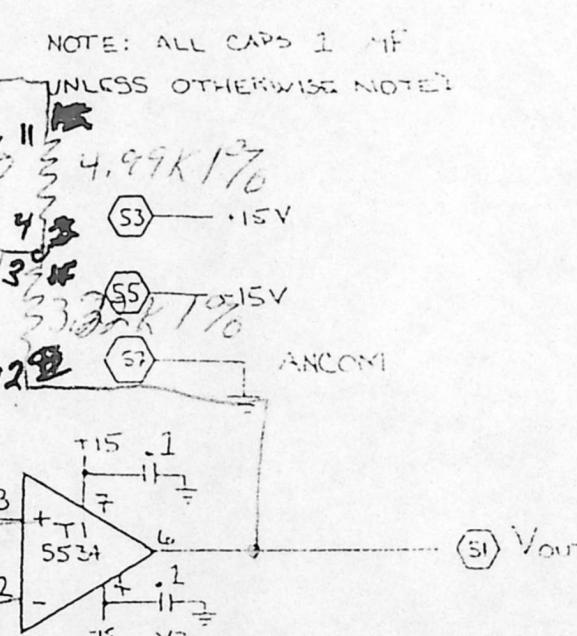
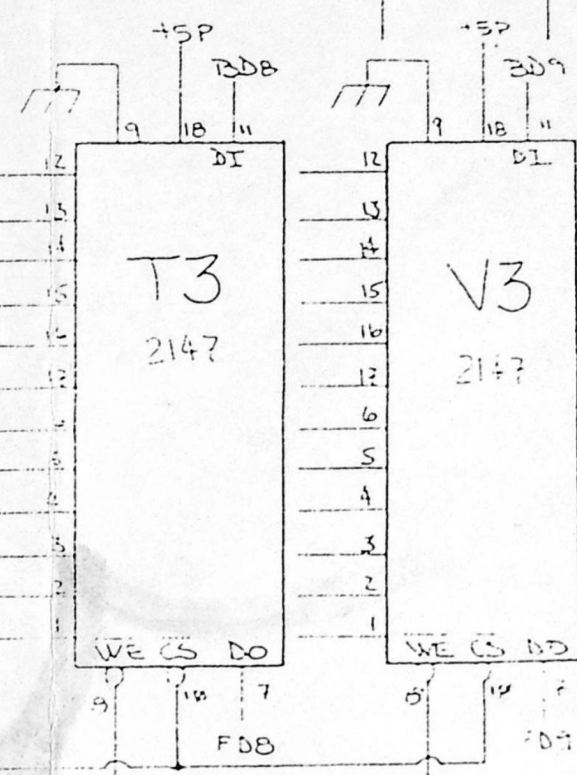
PCB	CIRC	
1	3	CIC-1-1
2	6	CIC-1-2
1	4	CIC-1-4
2	16	CIC-5
6		

RPU NEST 2

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
70	160 SPARE	BIN	MD	11	<u>+10</u>	HF	CIC-1-3
71	161 VERT CTR		MD				
72	162 H BLKG START		D				
73	163 H BLKG WIDTH		D				
78	170 MASK 1 RAD	OFF	D	12	<u>+10</u>	LF	CIC-1-2
79	171 MASK 2 RAD						
7A	172 MASK 3 RAD						
7B	173 HEIGHT						
80	200 MASK 2 SIN	ODD	MD	!@	<u>+10</u>	HF	CIC-1-1
81	201 MASK 2 COS						
82	202 MASK 3 SIN						
83	203 MASK 3 COS						
88	210						
	SPARE						
8F	217						

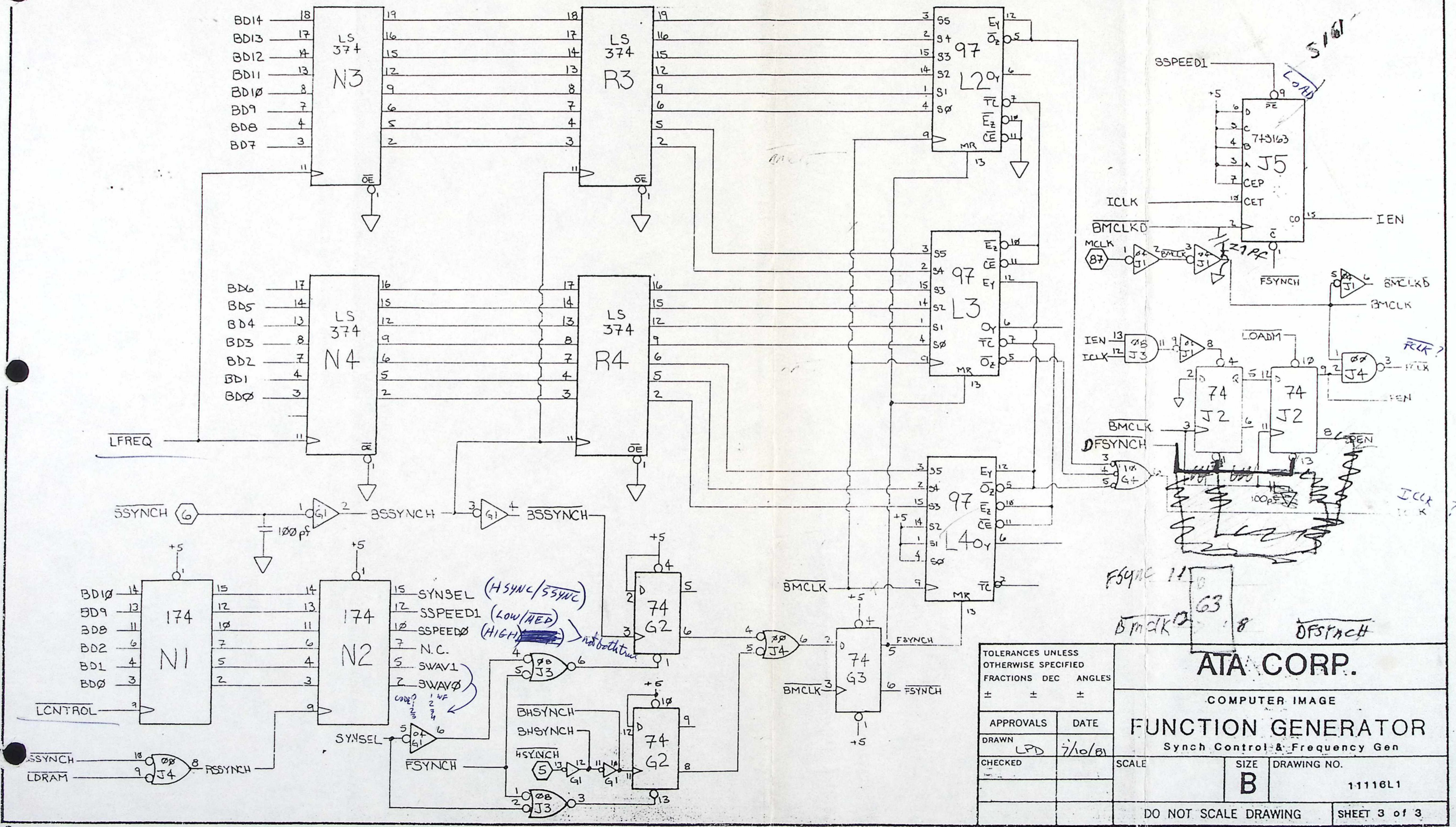
PCB	CIRC	
5	20	CIC-1-1
2	8	CIC-1-2
1	3	CIC-1-3
8		

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED		ATA CORP.	
FRACTIONS DEC ANGLES		COMPUTER IMAGE	
±	±	FUNCTION GENERATOR	
APPROVALS	DATE	D/A Output & WFM Storage	
DRAWN LDD	7/7/81		
CHECKED	SCALE	SIZE B	DRAWING NO
DO NOT SCALE DRAWING			SHEET 2 of 3

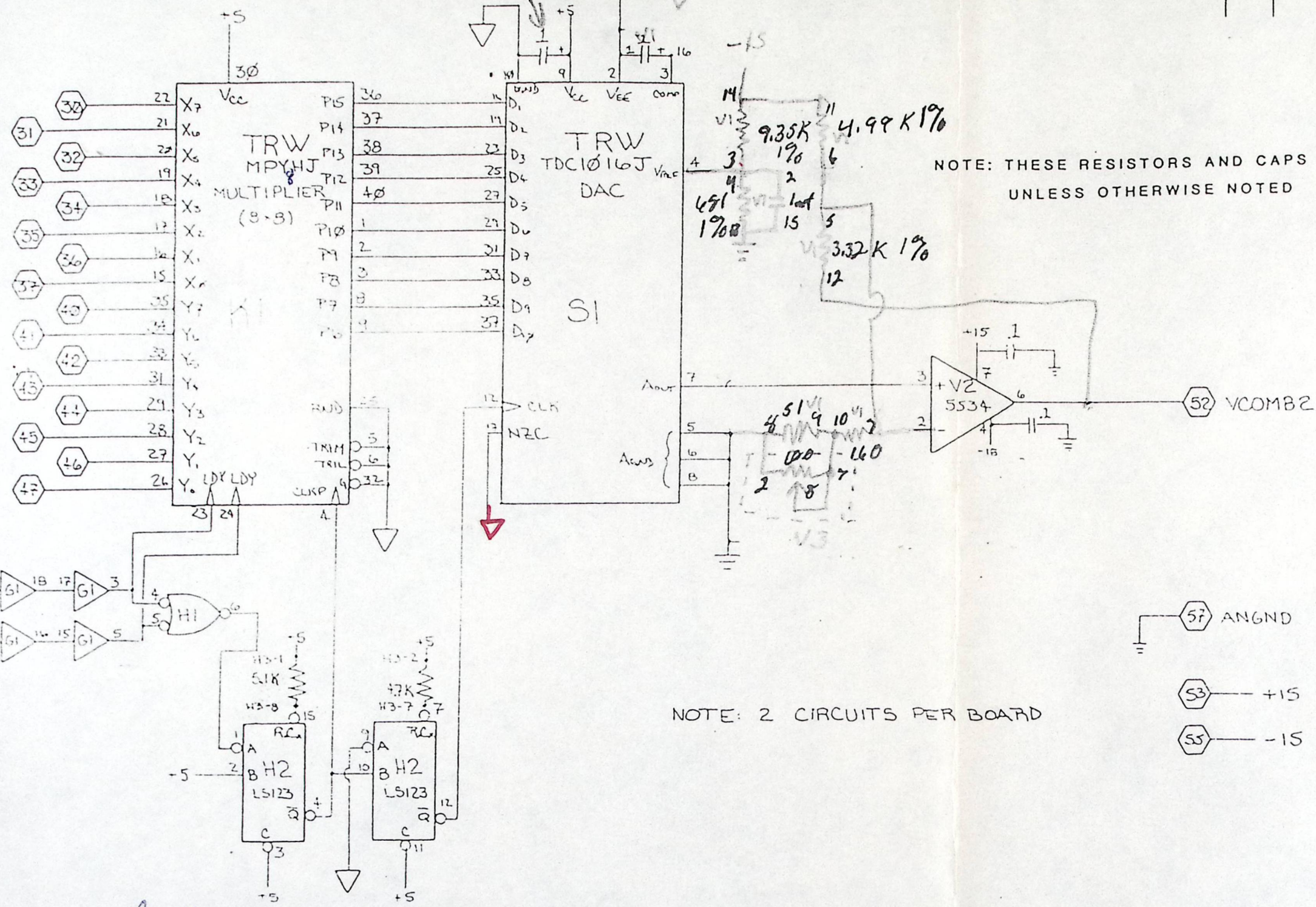
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
ATA CORP.			
COMPUTER IMAGE			
FUNCTION GENERATOR			
Synch Control & Frequency Gen			
APPROVALS	DATE	SCALE	SIZE
DRAWN	7/10/81		B
CHECKED			
DO NOT SCALE DRAWING		DRAWING NO.	
		1-1116L1	
		SHEET 3 of 3	

EMPTY
SECTION

FG2D7
FG2D6
FG2D5
FG2D4
FG2D3
FG2D2
FG2D1
FG2D0
FG3D7
FG3D6
FG3D5
FG3D4
FG3D3
FG3D2
FG3D1
FG3D0



NOTE: THESE RESISTORS AND CAPS AT LOCATION V1
UNLESS OTHERWISE NOTED

NOTE: 2 CIRCUITS PER BOARD

clock + Data timing very critical

NOTE: $\frac{1}{\square}$ DENOTES ISOLATED ANALOG GROUND

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
$\pm$	$\pm$	$\pm$	
ATA CORP.			
COMPUTER IMAGE			
FUNCTION GENERATOR			
Combiner Board			
APPROVALS	DATE	SCALE	SIZE
DRAWN LPD	7/28/81		B
CHECKED REV A	8/12/81		DRAWING NO. 010720L1
REV D	11/11/81		
DO NOT SCALE DRAWING			SHEET 2 of 2

+5P	F.1-20 K.1-30	H.4-16 N.1-16	H.3-2 N.2-16	H.3-4 N.3-16	H.2-16 S.2-9	H.1-14 S.1-9	K.2-30
-GNDP	F.1-10 S.1-10	H.4-8 <u>S.2-17</u>	H.2-8 <u>S.1-17</u>	H.1-7 S.1-16	K.2-32 S.2-10	K.1-32	<u>S.2-10</u>
+15	V.2-7	V.5-7	*Z0-53				
+5	H.4-2 H.2-11	H.4-3	H.4-11	H.3-1	H.3-3	H.2-2	H.2-3
-15	V.2-4	V.5-4	*Z0-55	<u>V.1-14</u>	<u>V.1-11</u>	<u>V.4-14</u>	<u>V.4-11</u>
-5	S.2-2 V.1-10	<u>S.1-2 OK</u> S.1-2 *Z0-64	<u>V.1-1</u> V.1-3	<u>V.4-1</u> V.1-1	V.1-10	V.4-3	V.4-1
-ANCOM	S.2-17 S.1-8 V.4-2 <u>V.3-5</u>	S.2-5 V.1-15 *Z0-57 <u>V.4-8</u>	S.2-6 V.1-15 V.4-13 <u>V.4-13</u> <u>V.4-15</u> <u>V.4-15</u>	S.2-8 V.1-8 V.1-13 <u>V.1-8</u>	S.1-17 V.4-13 <u>V.1-13</u>	S.1-5 V.4-15 <u>V.1-15</u> <u>V.3-2</u>	S.1-6 V.4-9
-GND	H.4-9 K.1-6	H.2-9	K.2-25	K.2-5	K.2-6	K.1-25	K.1-5

BLDAC1/	F.1-7	H.1-1	K.2-23
BLDAC21/	F.1-9	H.1-2	K.2-24
BLDAC23/	F.1-3	H.1-4	K.1-23
BLDAC3/	F.1-5	H.1-5	K.1-24
FG1D0	K.2-15	N.2-2	*Z0-97
FG1D1	K.2-16	N.2-3	*Z0-96
FG1D2	K.2-17	N.2-4	*Z0-95
FG1D3	K.2-18	N.2-5	*Z0-94
FG1D4	K.2-19	N.2-6	*Z0-93
FG1D5	K.2-20	N.2-7	*Z0-92
FG1D6	K.2-21	N.3-2	*Z0-91
FG1D7	K.2-22	N.3-1	*Z0-90
FG21D0	K.2-26	N.3-9	*Z0-107
FG21D1	K.2-27	N.3-10	*Z0-106
FG21D2	K.2-28	N.3-11	*Z0-105
FG21D3	K.2-29	N.3-12	*Z0-104
FG21D4	K.2-31	N.3-13	*Z0-103

FG21D5	K.2-33	N.3-14	*Z0-102
FG21D6	K.2-34	N.3-15	*Z0-101
FG21D7	K.2-35	N.2-9	*Z0-100
FG2D0	K.1-15	N.1-3	*Z0-37
FG2D1	K.1-16	N.1-4	*Z0-36
FG2D2	K.1-17	N.1-5	*Z0-35
FG2D3	K.1-18	N.1-6	*Z0-34
FG2D4	K.1-19	N.1-7	*Z0-33
FG2D5	K.1-20	N.2-1	*Z0-32
FG2D6	K.1-21	N.1-2	*Z0-31
FG2D7	K.1-22	N.1-1	*Z0-30
FG3D0	K.1-26	N.2-15	*Z0-47
FG3D1	K.1-27	N.1-9	*Z0-46
FG3D2	K.1-28	N.1-10	*Z0-45
FG3D3	K.1-29	N.1-11	*Z0-44
FG3D4	K.1-31	N.1-12	*Z0-43
FG3D5	K.1-33	N.1-13	*Z0-42
FG3D6	K.1-34	N.1-14	*Z0-41
FG3D7	K.1-35	N.1-15	*Z0-40
H.1-3	H.4-1	H.1-3	
H.1-6	H.2-1	H.1-6	
H.2-12	H.2-12	S.1-12	
H.2-4	H.2-4	H.2-10	K.1-4
H.3-5	H.4-7	H.3-5	
H.3-6	H.4-15	H.3-6	
H.3-7	H.3-7	H.2-7	
H.3-8	H.3-8	H.2-15	
H.4-12	H.4-12	S.2-12	
H.4-4	H.4-4	H.4-10	K.2-4

K.1-1	K.1-1	S.1-29
K.1-2	K.1-2	S.1-31
K.1-3	K.1-3	S.1-33
K.1-36	K.1-36	S.1-16
K.1-37	K.1-37	S.1-19
K.1-38	K.1-38	S.1-23
K.1-39	K.1-39	S.1-25
K.1-40	K.1-40	S.1-27
K.1-8	K.1-8	S.1-35
K.1-9	K.1-9	S.1-37
K.2-1	K.2-1	S.2-29
K.2-2	K.2-2	S.2-31
K.2-3	K.2-3	S.2-33
K.2-36	K.2-36	S.2-16
K.2-37	K.2-37	S.2-19
K.2-38	K.2-38	S.2-23
K.2-39	K.2-39	S.2-25
K.2-40	K.2-40	S.2-27
K.2-8	K.2-8	S.2-35
K.2-9	K.2-9	S.2-37
LDAC1	F.1-14	F.1-13
LDAC1/	F.1-6	*Z0-98
LDAC21	F.1-12	F.1-11
LDAC21/	F.1-8	*Z0-108
LDAC23	F.1-18	F.1-17
LDAC23/	F.1-2	*Z0-38
LDAC3	F.1-16	F.1-15
LDAC3/	F.1-4	*Z0-48
S.1-4	S.1-4	V.1-1

V.1-2 V.1-3

V.3-8

V.1-4

S.1-7	S.1-7	V.2-3	
S.2-4	S.2-4 S.2-4 OK	V.4-2 V.4-2	V.6-2 V.4-3 V.4-4
S.2-7	S.2-7	V.5-3	
V.1-12	V.1-12	V.1-11	V.2-2
V.1-14	V.1-14	V.3-2	
V.1-16	S.1-3	V.1-16 V.1-16 OK	
V.1-6	V.1-6	V.3-6 V.1-5 V.1-7 V.2-2	
V.1-7	V.1-7	V.5-4	
V.1-8	V.1-8	V.3-5	
V.3-7	V.1-9 V.1-9	V.3-7 V.1-10 V.3-8 V.3-7	
V.4-12	V.4-12	V.4-11 V.5-2	
V.3-4	V.3-4	V.3-6 V.4-9 V.4-10	
V.1-14	V.4-14	V.6-2	
V.4-16	S.2-3	V.4-16	
V.4-6	V.4-6	V.4-5 V.4-6 V.4-7 V.5-2	
V.4-7	V.4-7	V.6-4	
V.4-8	V.4-8	V.6-5	
V.6-7	V.4-1	V.6-7	
VCOMB1	V.4-5 V.4-12	V.5-6	*Z0-51
VCOMB2	V.1-5 V.1-12	V.2-6	*Z0-52

TOTAL NUMBER OF WIRE WRAPS: 396

TOTAL PINS USED: 301

~~*INSTRUCTIONS AND NOTES FOR PREPERATION AND WIREWRAP OF THE
COMPUTER IMAGE FUNCTION GENERATOR*~~

PREPERATION FOR WIREWRAPPING

1. REMOVE PINS ACCORDING TO ASSEMBLERS LAYOUT SHEET
2. CUT GROUND PLANE ACCORDING TO ASSEMBLERS LAYOUT FIG. 1
3. WITH KROY LABELING SYSTEM LABEL ALL LOCATIONS ACCORDING TO ASSEMBLERS LAYOUT
4. SOLDER 18 GUAGE BUSWIRE FROM PIN *Z0-62 TO *Z0-63 TO DIGITAL GROUNDPLANE AND FROM PIN *Z0-122 TO *Z0-123 TO DIGITAL GROUNDPLANE

** YOU ARE NOW READY TO GOTO WIREWRAP LIST, GOOD LUCK AND HAPPY WIRING **
**
** REFER TO ALL SOLDER AND WIRING NOTES WHILE FOLLOWING WIREWRAP LIST **

SD.1-1 SOLDER .1 uf CAPACITORS TO PINS ON WIREWRAPLIST DISPEGUARD THE X INFRONT OF PIN POSITIONS. SOLDER OTHER LEG OF CAPACITORS DIRECTLY TO THE DIGITAL GROUNDPLANE.

SD.1-2 CAPS1 ARE .1 uf CAPACITORS ONE LEG IS SOLDERED TO THE PIN LISTED THE OTHER LEG IS SOLDERED DIRECTLY TO THE ISOLATED GROUNDPLANE. CAPS2 ARE 1mf. CAPACITORS ONE LEG IS SOLDERED TO THE PIN LISTED THE OTHER LEG IS SOLDERED DIRECTLY TO THE ISOLATED GROUNDPLANE

SD.1-3 CAP3 AND CAP4 ARE 1 uf CAPACITORS. CAP3 IS SOLDERED WITH ONE LEG T.2-2 AND THE OTHER TO T.2-3 CAP4 IS SOLDERED WITH ONE LEG TO T.2-9 AND THE OTHER LEG TO T.2-10

SD.2-1 WITH A SIX INCH LENGTH OF 26 GUAGE WIRE, STRIP INSULATION FROM WIRE AND WRAP TO PINS LISTED INSERT OTHER END OF WIRE THRU NEAREST HOLE IN BOARD AND SOLDER DIRECTLY TO VOLTAGE PLANE (VCC).

SD.2-2 WITH A SIX INCH LENGTH OF 26 GUAGE WIRE, STRIP WIRE AND WRAP ONE END OF WIRE TO PINS LISTED AND SOLDER OTHER END DIRECTLY TO THE DIGITAL GROUNDPLANE.

SD.2-3 WITH 18 GUAGE BUSWIRE SOLDER TO BUS PIN *Z0-57 SLEEVE WIRE AND SOLDER OTHER END DIRECTLY TO ISOLATED GROUNDPLANE

PP.1-1 ALL WIRES MUST BE WRAPPED DIRECTLY TO A GROUND PIN

PP.1-2 ALL WIRES MUST BE WRAPPED DIRECTLY TO A VOLTAGE PIN

PP.1-3 ALL WIRES MUST BE WRAPPED TO THE ISOLATED GROUND PINS.

PP.1-4 GROUND WIRE OF TWISTED PAIR MUST USE ISOLATED GROUND

TWIST STANDS FOR TWISTEDPAIR WIRE WRAP ONE END OF YELLOW WIRE TO CLOSEST GROUND PIN WRAP ONE END OF BLUE WIRE TO PIN LISTED. TWIST WIRES TOGETHER AND WRAP BLUE WIRE TO NEXT PIN LISTED WRAP REMAINING WIRE TO GROUND PIN. FOLLOW TWISTED PAIR ROUTING DIAGRAMS.

ROUTE REFERS TO A ROUTING DIAGRAM

***** IMPORTANT *****
***** DO NOT DEVIATE FROM WIREWRAP LIST AND ROUTING DIAGRAMS *****

Models: TDC1016J-8
TDC1016J-9
TDC1016J-10

PRELIMINARY INFORMATION

The TRW TDC1016J-8/9/10 bit D/A converters are capable of converting a digital signal into an analog voltage at the rate of 20 megasamples per second (MSPS). No external input register, deglitching, or resampling is needed. No operational amplifier or buffer is required at the analog output.

All parts have 10 bits of active digital input. Three accuracy grades are offered: 8, 9, 10 bits. Simply grounding the V_{CC} terminal causes the inputs to become ECL compatible.

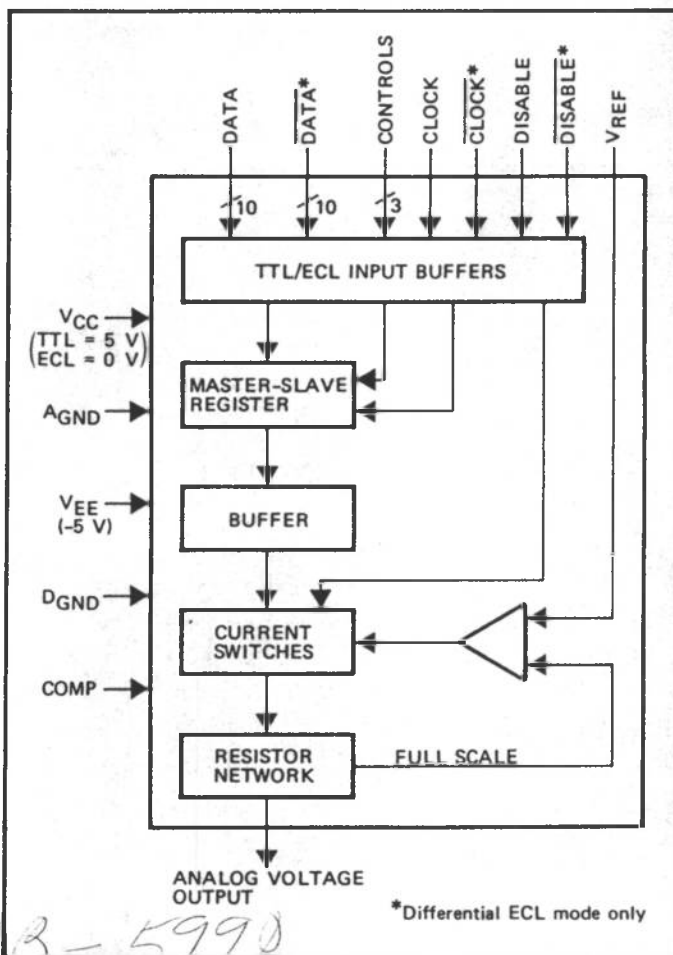
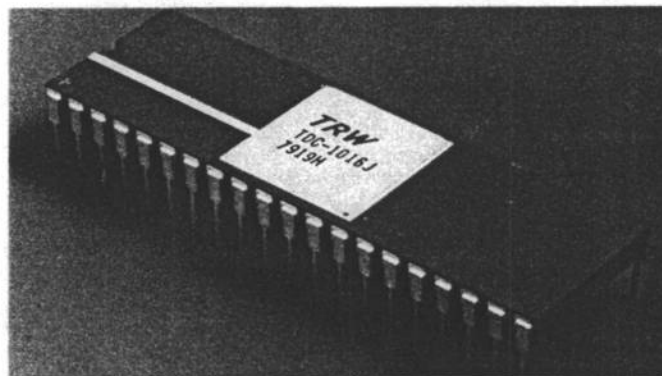
The TDC1016J is patented (U.S. Patent No. 3283170) with other patents pending.

FEATURES

- 8, 9, and 10 bit accuracy
- 20 MSPS
- Voltage output
- ECL or TTL inputs (only -5.0V supply required for ECL mode)
- Single ended or differential ECL inputs
- All data registered on chip
- No deglitching circuit required
- Output disable capability
- Differential phase: 0.5°
- Differential gain: 1.0%
- Binary or two's complement input
- Zero and full scale control for easy calibration
- Data inversion control
- Monolithic, bipolar
- 40 pin ceramic DIP
- 0.6 W power dissipation

APPLICATIONS

- Video data conversion
3X or 4X NTSC color
3X or 4X PAL color
- Color/B&W graphics
- CRT displays
- Waveform/test signal generation



LSI D/A CONVERTERS

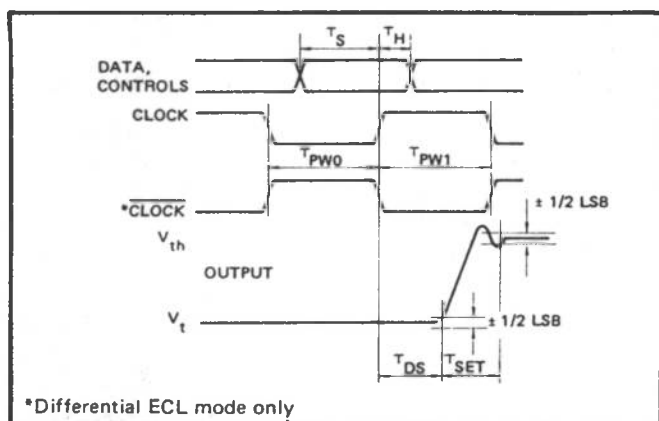


Figure 1. Timing Diagram

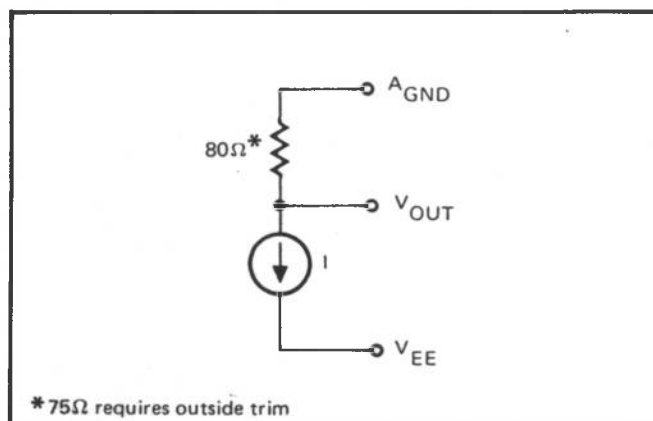


Figure 2. Analog Output Equivalent Circuit, TTL & ECL Mode

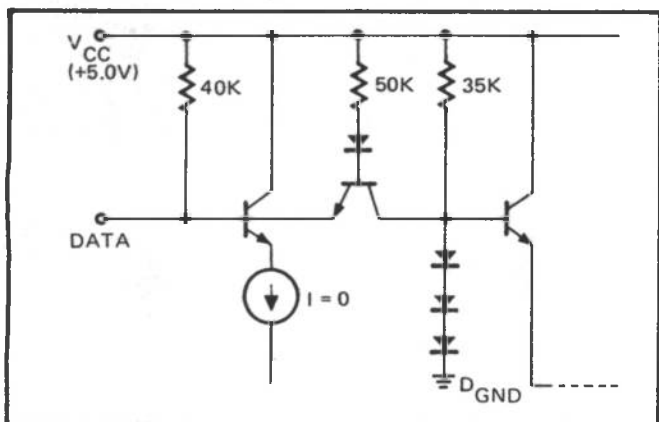


Figure 3. Digital Input Equivalent Circuit, TTL Mode

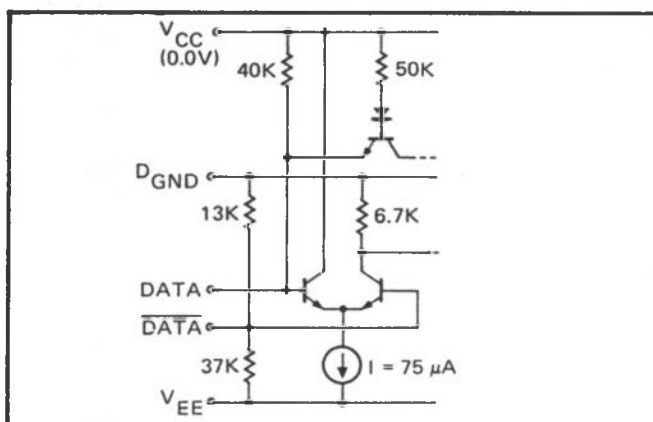


Figure 4. Digital Input Equivalent Circuit, ECL Mode

Performance characteristics, over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TDC1016J-8			TDC1016J-9			TDC1016J-10			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8			9			10		Bits
			0.39			0.19			0.10		%
Linearity error	0 to 20 MSPS conversion rate			0.20			0.10			0.05	%
Dynamic range	$Z_L > 10K\Omega$	0.8	1.0	1.2	0.8	1.0	1.2	0.8	1.0	1.2	V
	$Z_L = 75\Omega$	0.4	0.5	0.6	0.4	0.5	0.6	0.4	0.5	0.6	V
Output impedance	Resistance	75	80*	85	75	80*	85	75	80*	85	Ω
	Capacitance		5			5			5		pF
Differential phase			0.5			0.5			0.5		Deg
Differential gain			1.0			1.0			1.0		%

*75Ω requires outside trim

LSI D/A CONVERTERS

SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage, V_{CC}	-0.5 to +7.0 V
V_{EE}	+0.5 to -7.0 V
Input voltage, digital	-7.0 to +7.0 V
analog ground	-1.0 to +1.0 V
reference	-7.0 to +7.0 V
Output voltage	-2.0 to +2.0 V
Temperature, operating, ambient	-55 to +150°C
junction	+175°C
lead, soldering (10 seconds)	+300°C
storage	-65 to +150°C

Recommended operating conditions

PARAMETER	TTL			ECL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , Supply voltage	+4.75	+5.0	+5.25	-0.25	0	+0.25	V
V_{EE} , Supply voltage	-4.75	-5.0	-5.25	-4.75	-5.0	-5.25	V
V_{REF} , Reference voltage	-0.8	-1.0	-1.2	-0.8	-1.0	-1.2	V
τ_{PW1} , τ_{PW0} , pulsewidth (see Figure 1)	15			15			nsec
τ_S , Input register setup time	20			20			nsec
τ_H , Input register hold time	0			0			nsec
T_A , Operating ambient temperature range	0		+70	0		+70	°C
Compensation capacitor (between COMP and V_{EE})	1.0			1.0			μF

Electrical characteristics over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TTL			ECL			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
Power Supply								
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		10	15				mA
I_{EE} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		100	120		100	120	mA
Analog								
I_{REF} Reference input current	$V_{EE} = \text{MAX}, V_{REF} = -1.0 \text{ V}$		0.1			0.1		μA
V_{OFS} Full scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$	-0.970	-1.0	-1.030	-0.970	-1.0	-1.030	V
V_{OZS} Zero scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$			10			10	mV
Digital								
V_{IH} High level input voltage		+2.0			-1.105			V
V_{IL} Low level input voltage				+0.8			-1.475	V
I_{IH} High level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 2.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -0.81 \text{ V}$			75			100	μA
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 0.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -1.85 \text{ V}$			-0.75			-0.75	mA

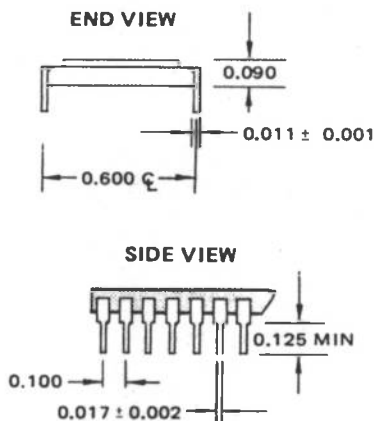
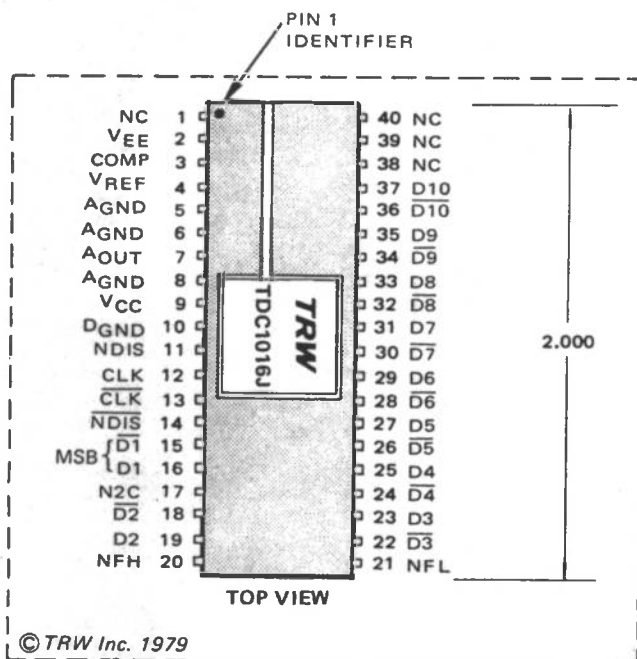
* $V_{CC}, V_{EE}, T_A = \text{TYP}$

Switching characteristics over recommended operating temperature and supply ranges

PARAMETER	TEST CONDITIONS	TTL/ECL			UNIT
		MIN	TYP	MAX	
F_C Maximum conversion rate		20			MSPS
τ_{DOFF} Ladder turnoff delay	$R_L = 75\Omega$			30	nsec
τ_{DON} Ladder turnon delay	$R_L = 75\Omega$			30	nsec
τ_{DS} Data turnon delay, Figure 1	$R_L = 75\Omega$		15		nsec
τ_{SET8} Transient settling time, Figure 1, 0.20%	$R_L = 75\Omega$		20		nsec
τ_{SET9} 0.10%			25		nsec
τ_{SET10} 0.05%			30		nsec
Output transient (glitch), energy amplitude	$R_L = 75\Omega$, midscale		100		pV-sec
			20		mV

LSI D/A CONVERTERS

PACKAGE INFORMATION TDC1016J-8/9/10



THERMAL RESISTANCE DATA

Junction to case	$\theta_{JC} \approx 25^\circ \text{ C/W}$
Case to ambient	$\theta_{CA} \text{ (Still air)} \approx 25^\circ \text{ C/W}$
Case to ambient	$\theta_{CA} \text{ (5 ft/sec airflow)} \approx 15^\circ \text{ C/W}$

NOTES: DIMENSIONS IN INCHES.
UNUSED PINS CAN BE LEFT OPEN.

INPUT CODING

DISABLE NDIS	TWO'S COMPLEMENT N2C	FORCE HIGH NFH	FORCE LOW NFL	INPUT		OUTPUT	FUNCTIONAL DESCRIPTION
				MSB	LSB		
1	1	1	1	1111111111	0000000000	0.0V -1.0V	Default controls
0	x	x	x	xxxxxxxxxx		0.0V	Output disable
1	x x	0 1	1 0	xxxxxxxxxx xxxxxxxxxx		0.0V -1.0V	Force high Force low
1	1	0	0	1111111111	0000000000	-1.0V 0.0V	Inverted
1	0	1	1	0111111111	1000000000	0.0V -1.0V	Two's complement
1	0	0	0	0111111111	1000000000	-1.0V 0.0V	Two's complement inverted

x - Don't care

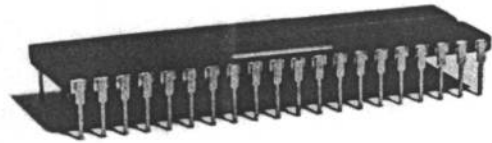
TRW reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of TRW Inc. or others.

The MPY LSI multipliers are high speed, TTL LSI devices. They are n-by-n parallel array multipliers with double precision outputs. Their low power and high performance characteristics are the result of a proven method developed and patented by TRW (U.S. Patent No. 3,900,724). Fundamental TTL devices used to produce the MPY-LSI were also developed and patented by TRW (U.S. Patent No. 3,283,170). The major multiplier array logic achieves speed-power performance of less than 1 picojoule per equivalent gate.

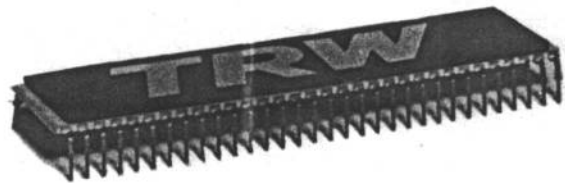
Four input/output registers are used in the MPY LSI multipliers. These registers are D-type flip-flops with a single phase TTL clock.

Applications for MPY LSI multipliers include digital processing and high speed multiplication for fast Fourier transforms. They are ideal for extending the capabilities of mini/microcomputers, permitting hardware multiplication for increased computational speed.

They have a better than 2-to-1 speed-power improvement over the MPY AJ series multipliers.



MPY-8HJ



MPY-12HJ, MPY-16HJ, and MPY-24HJ

FEATURES

- n-by-n parallel array multiplier, n = 8, 12, 16, or 24
- Double precision product
- 45 to 200 nsec typical multiply time
- Much lower power/less space than MSI equivalent multipliers
- Includes input/output registers
- Single chip, bipolar TTL technology
- Single bus or multiport operation
- Radiation hard
- Three-state outputs
- Single power supply, +5V

NEW FEATURES OF HJ SERIES

- Higher speed/lower power
- Zero-nanosecond register hold time
- Two's complement, unsigned magnitude, or mixed-mode multipliers (all except MPY-8HJ)
- Easily expandable for larger array multiplication
- Worst case specs across full voltage and temperature ranges
- Controllable, transparent product registers (all except MPY-8HJ)
- Shift/normalize product capability (MPY-24HJ)
- Pin-compatible with AJ series multipliers

GENERAL INFORMATION

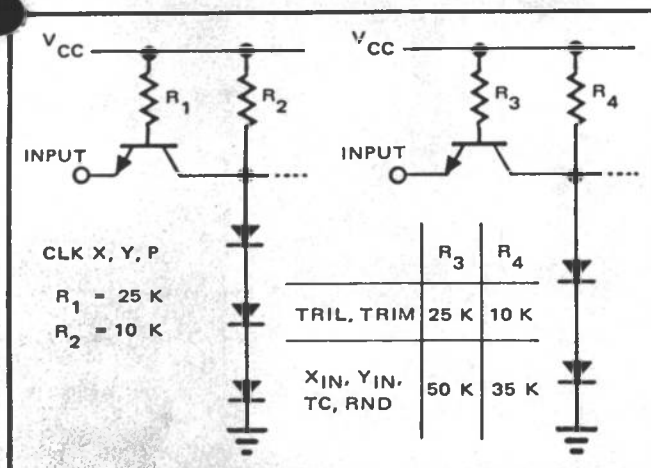


Figure 1. Equivalent Input Schematics

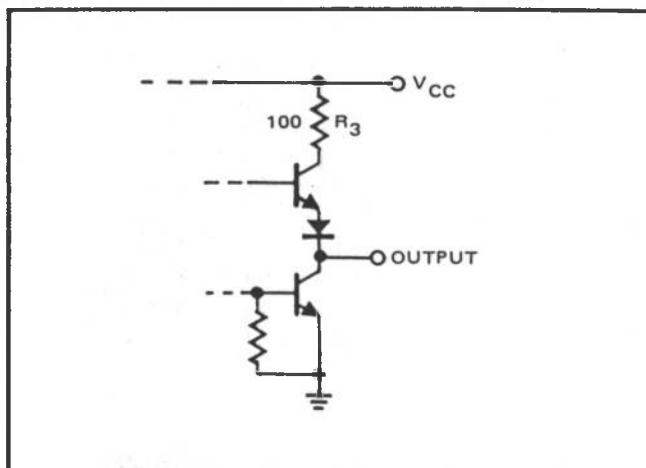


Figure 2. Output Schematic

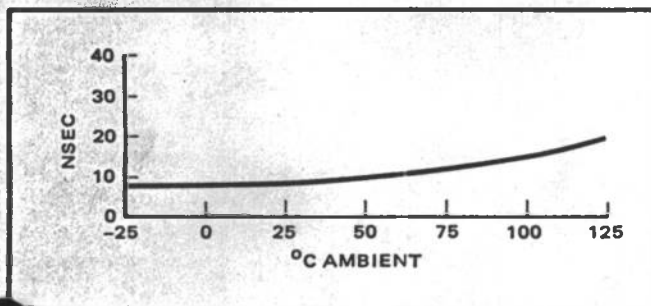


Figure 3. Typical Setup Time

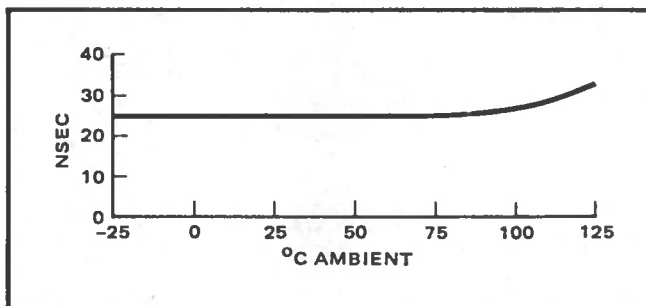


Figure 4. Typical Three-State Delay, Output Delay

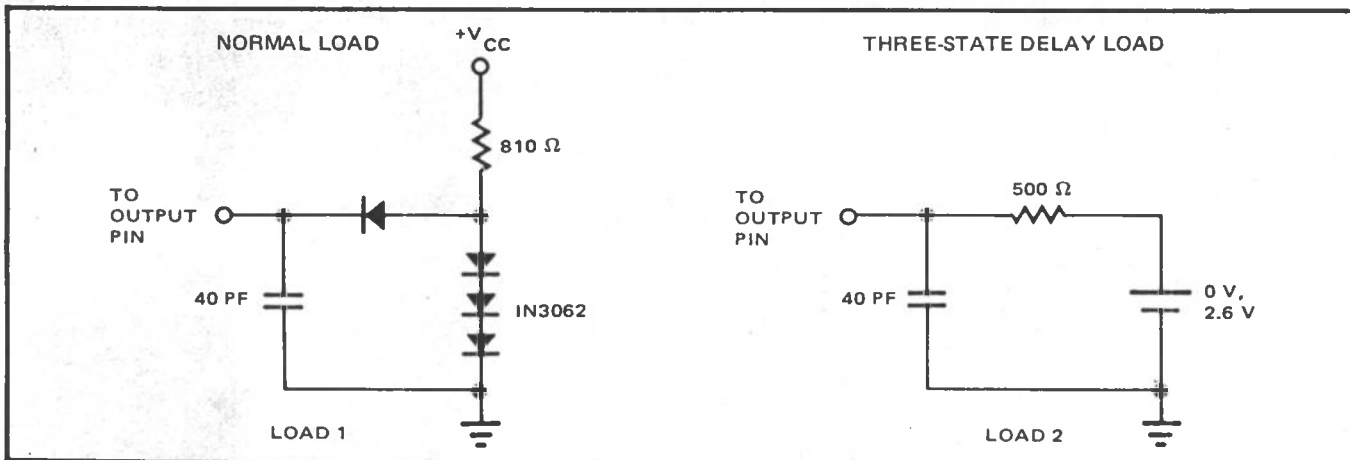


Figure 5. Test Loads for Delay Measurements

SOCKET INFORMATION

TYPE	40 PIN	64 PIN
Wire wrap	Excel 800B-003-40	Excel 800B-003-64
Solder tail-tin plate	Cambion 703-4040-01-04-12	Cambion 703-4064-01-04-12
Solder tail-gold plate	Robinson Nugent ICN-406-S5-G	Robinson Nugent ICN-649-S5-G
Zero insertion force	Textool 240-3346-00-0605	Textool 232-2601-00-0605 (2 Required)

GENERAL SPECIFICATIONS

Absolute maximum ratings (above which the useful life may be impaired)

Supply voltage	-0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range (T _{case})	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

Part Numbers

Commercial	Military
MPY-8HJ	MPY-8HJM
MPY-8HJ-1	—
MPY-12HJ	MPY-12HJM
MPY-16HJ	MPY-16HJM
MPY-24HJ	MPY-24HJM

Recommended operating conditions

	COMMERCIAL			MILITARY			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
High-level output current, I _{OH}			-0.4			-0.4	mA
Low-level output current, I _{OL}			4.0			4.0	mA
Clock pulse width, t _{PW} (measured at 1.5 V level)	25			30			nsec
Input register setup time, t _S (see Figure 6)	25			30			nsec
Input register hold time, t _H (see Figure 6)	0			0			nsec
Operating temperature (T _{ambient} for commercial, T _{case} for military)	0		70	-55		125	°C

Electrical characteristics over recommended temperature range (except as otherwise noted)

PARAMETER	TEST CONDITIONS	COMMERCIAL			MILITARY			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
V _{IH} High-level input voltage		2.0			2.0			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{OH} High-level output voltage	V _{CC} = MIN I _{OH} = -0.4 mA	2.4	2.7		2.4	2.7		V
V _{OL} Low-level output voltage	V _{CC} = MIN I _{OL} = 4.0 mA		0.3	0.5		0.3	0.5	V
I _{IH} High-level input current	V _{CC} = MAX V _{IH} = 2.4			75			75	μA
I _{IL} Low-level input current	V _{CC} = MAX V _{IL} = 0.4			-0.4			-0.4	mA
I _{IH} Clocks*, three-states—high level input current	V _{CC} = MAX V _{IL} = 2.4			75			75	μA
I _{IL} Clocks*, three-states—low level input current	V _{CC} = MAX V _{IL} = 0.4			-1.0			-1.0	mA

*NOTE: Clock P is two equivalent clock loads.

Switching characteristics across V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP**	MAX		UNIT
			COMMERCIAL	MILITARY	
Output delay t _D	Load 1 (see Figure 5)	25	35	40	nsec
Three state output delay Output enable, t _{ENA} . Output disable, t _{DIS}	Load 2 (see Figure 5)	25	35	40	nsec

**NOTE: At V_{CC} = 5.0 V, T_A = 25°C.

MPY-8HJ

8 X 8 BIT PARALLEL MULTIPLIER

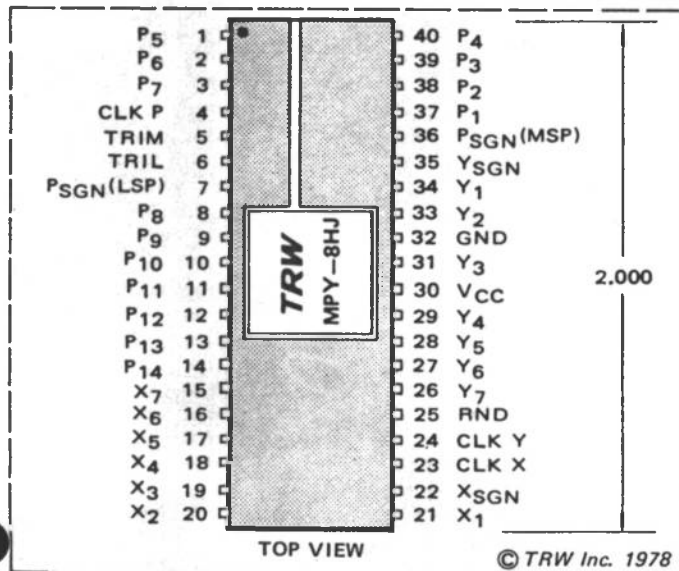
The MPY-8HJ multiplier is a high speed, TTL LSI device. It is a parallel two's complement multiplier with double precision output. It can be plugged into an MPY-8AJ socket, and be functionally equivalent. However, this newer multiplier has positive setup and zero hold times, which reduces system clocking complexity in many applications. Also, the RND control is now a registered input, making its timing and usage more convenient.

Four input/output registers are used in the MPY-8HJ multipliers. These registers are D-type flip-flops with a single phase TTL clock.

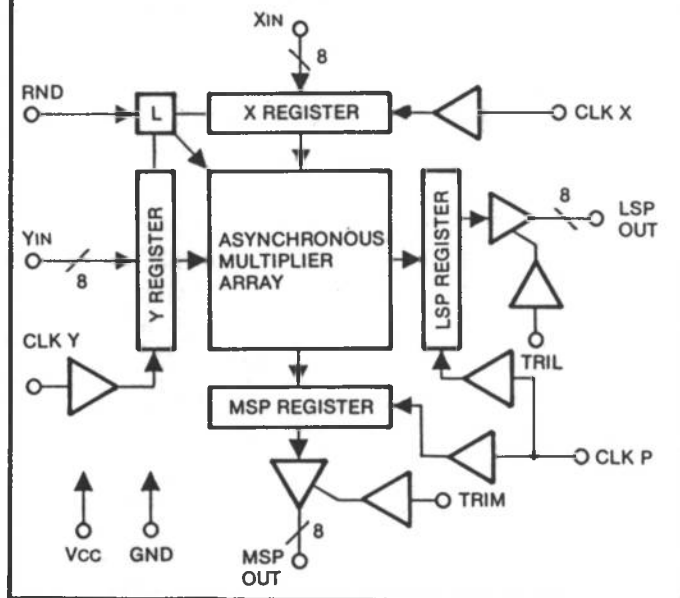
Applications for the MPY-8HJ multipliers include digital processing and high speed multiplication for fast, nonrecursive filters. They are ideal for extending the capabilities of mini/microcomputers, permitting hardware multiplication for increased computational speed, and are particularly useful for video processing.

FEATURES

- 8-by-8 parallel, two's complement multiplier
- Double precision product
- 65 nsec typical multiply time (MPY-8HJ)
- 45 nsec typical multiply time (MPY-8HJ-1)
- Much lower power than MSI equivalent multipliers
- Includes input/output positive edge-triggered registers
- Single chip, bipolar technology
- Single bus or multiport operation
- Radiation hard
- TTL input and output
- Three state outputs
- Single power supply, +5V
- 40 pin dual in-line package
- Pin compatible with MPY-8AJ
- Zero hold time on input registers



MPY-8HJ LOGICAL BLOCK DIAGRAM



CONTROLS

(Positive logic unless otherwise noted)

CLK X - X_{IN} Register Clock

CLK Y - Y_{IN} Register Clock

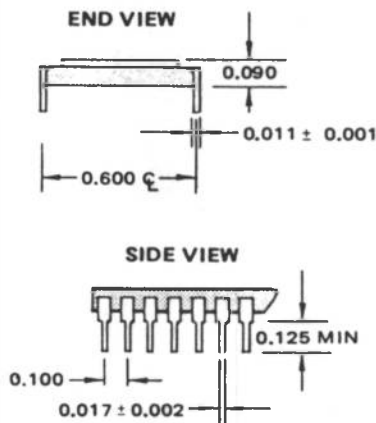
CLK P - Product Registers Clock

TRIL - LSP Three-State Control,
TRIM - MSP Three-State Control,
LOGIC 0 = Enable, LOGIC 1 = Disable

RND (LOGIC 1) - Adds 2^{-8} to product (fractional two's complement field - See Page 5 for I/O Format)

RND Latch is strobed by (CLK X or CLK Y)

PACKAGE INFORMATION



NOTE
DIMENSIONS IN INCHES

THERMAL CHARACTERISTICS

θ_{CA} (Still air) = 25°C/W

θ_{CA} (300 cfm) = 15°C/W

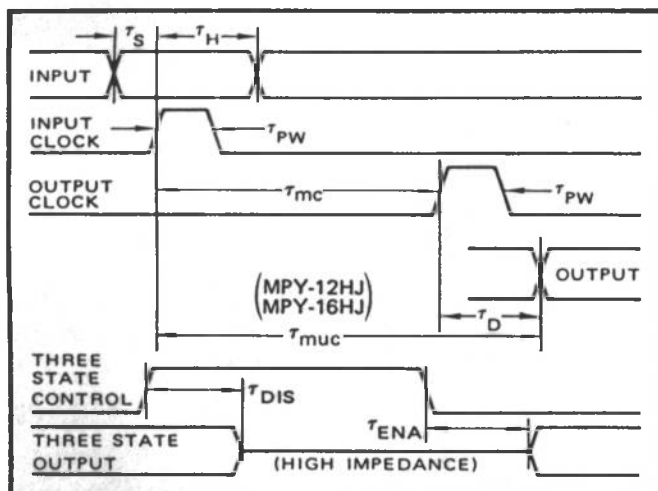


Figure 6. Timing Diagram

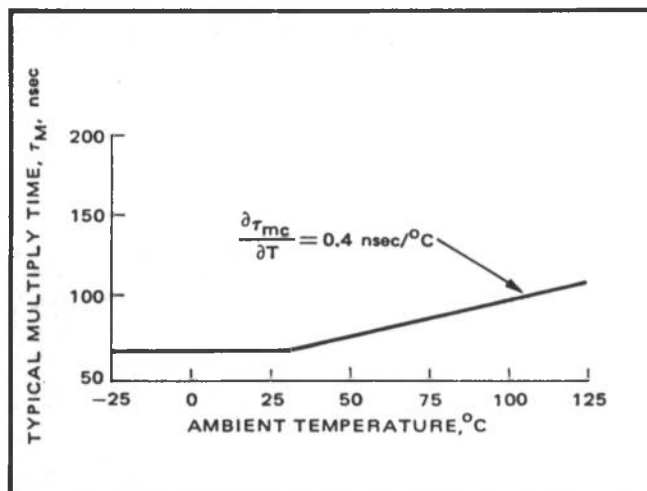
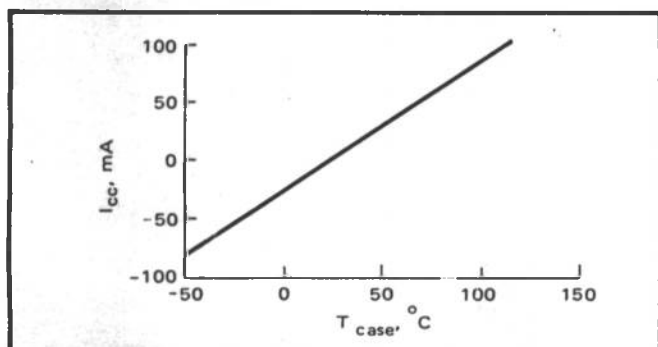
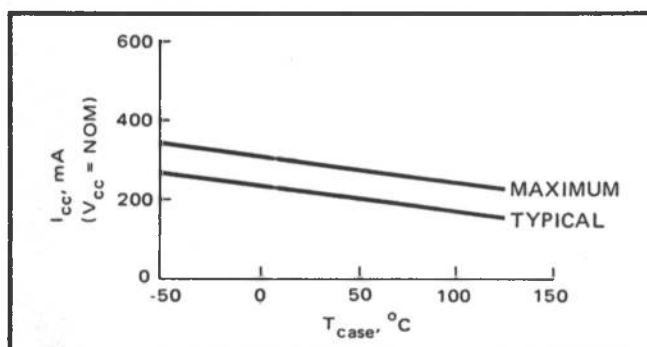


Figure 7. Multiply Time Versus Temperature


Figure 8. T_{ambient} Versus T_{case}

Figure 9. I_{CC} Versus T_{case}

Electrical and switching characteristics over recommended V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP*	MAX		UNIT
			COMMERCIAL	MILITARY	
MPY-8HJ Multiply time, τ_{mc}	See Figures 6, 7	65	90	115	nsec
MPY-8HJ-1 τ_{mc}	See Figure 6	$T_A = 60^\circ\text{C}$	45	—	nsec
		$T_A = 70^\circ\text{C}$	45	—	nsec
Supply current I_{CC}	See Figure 9	200	270	330	mA

* NOTE: At $V_{\text{CC}} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$

INPUT/OUTPUT FORMAT FOR FRACTIONAL TWO'S COMPLEMENT FIELD

X_{IN}								Y_{IN}							
X SGN	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y SGN	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}
								-2^0	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
P SGN	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P SGN	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}
MSP								LSP							

An overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . (-1 base 10) with itself, yielding a result of the same number, i.e., $(-1)_{10} * (-1)_{10} = (-1)_{10}$

MPY-12HJ and MPY-16HJ

12 X 12 and 16 X 16 BIT PARALLEL MULTIPLIERS

The MPY-12HJ and MPY-16HJ multipliers are high speed TTL compatible LSI devices. They are N-by-N parallel array multipliers with double precision or single precision (uniform rounded or truncated) outputs.

The input registers are positive edge-triggered latches. The output latches are similarly positive edge-triggered latches, with a feedthrough control line, which allows the user to bypass the registers completely, making them asynchronous. If the output clocks are disabled, then the feedthrough control can be used to convert the output registers to level latches.

Applications for these multipliers include high speed digital signal processing, such as Fourier transforms, FIR and IIR filters, and linear predictive algorithms. They are ideal for upgrading the capabilities of mini and microcomputers, permitting hardware multiplication for increased computational speed at low cost. They can also be added on a retrofit basis to older signal processors, decreasing system power and size, while increasing reliability and (in many cases) system throughput.

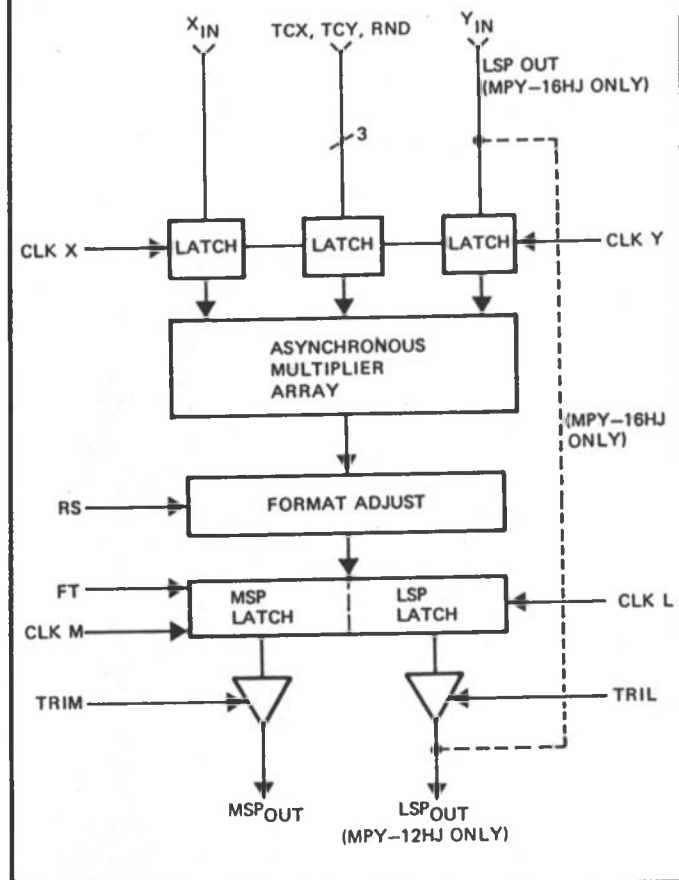
These multipliers can be plugged into MPY-12AJ and MPY-16AJ sockets, and be functionally equivalent. However, these newer multipliers have positive setup and zero hold times, which reduces system clocking complexity in many applications. The RND control is now a registered input, making its timing and usage more convenient.

The multipliers can operate with two's complement, unsigned magnitude, and mixed mode input formats. As such, they are ideal for expansion into larger multipliers, such as 32 by 32 bits, or 36 by 36 bits.

FEATURES

- 12 x 12 (MPY-12HJ) or 16 x 16 (MPY-16HJ) parallel array multiplier
- Double precision output
- 80 nsec (MPY-12HJ), 100 nsec (MPY-16HJ) multiply time
- Two's complement, unsigned magnitude, or mixed mode multiplies
- Positive edge-triggered input latches
- Output latches positive edge-triggered or transparent
- Three-state outputs
- Pin compatible with MPY-12AJ or MPY-16AJ
- Two output formats

MPY-12HJ and MPY-16HJ LOGIC BLOCK DIAGRAM



CONTROLS

(Positive logic unless otherwise noted)

CLK X — X_{IN} Register Clock

CLK Y — Y_{IN} Register Clock

CLK L — LSP Register Clock

CLK M — MSP Register Clock

TRIL — LSP Three-State Control,

TRIM — MSP Three-State Control,

RS — Right Shift MSP word down 1 bit, removes LSP SIGN bit.

FT (Feedthrough) — Makes output latch transparent

TCX, TCY — Denotes respective input words as two's complement (logic 1) or magnitude (logic 0) data format (registered control inputs strobed by respective clocks)

ROUND — ADDS 1 to MSB bit of LSP word, regardless of shift position (registered control input strobed by [CLK X or CLK Y]).

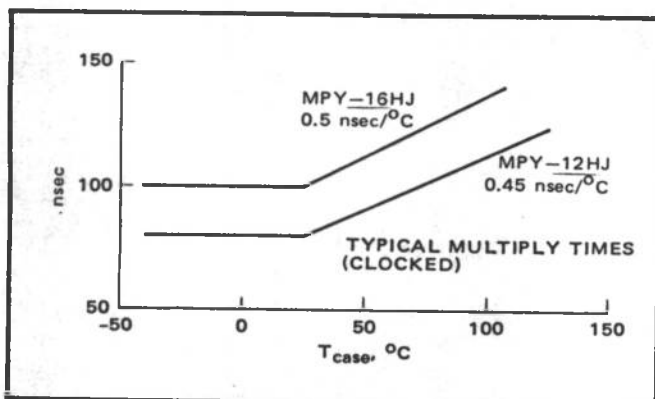


Figure 10. Multiply Time Versus Temperature

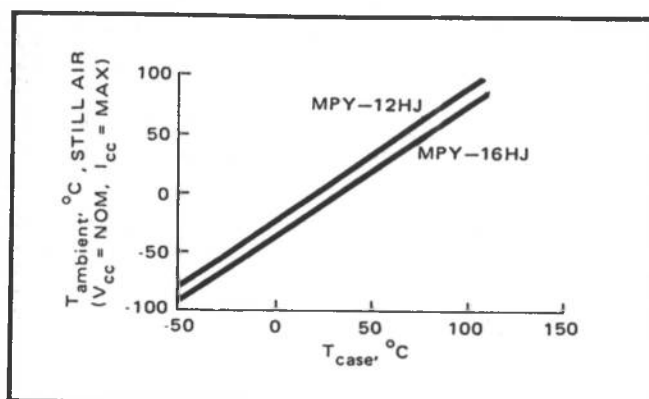


Figure 11. Tambient Versus Tcase

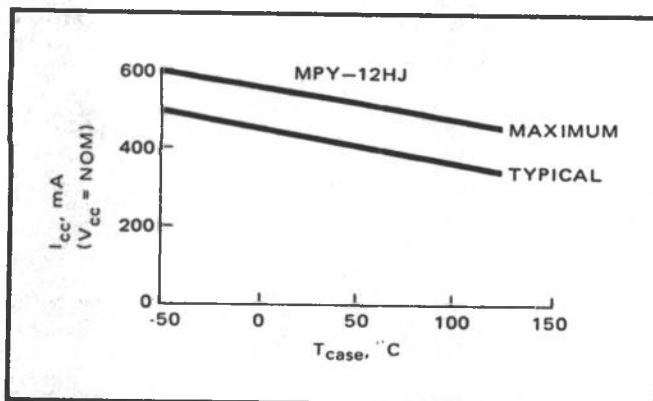


Figure 12. ICC Versus Tcase

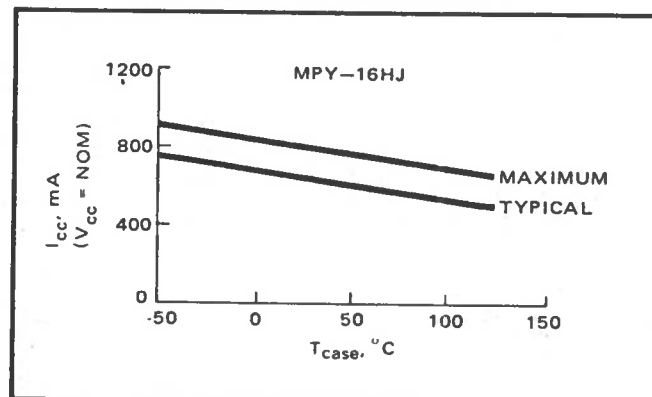


Figure 13. ICC Versus Tcase

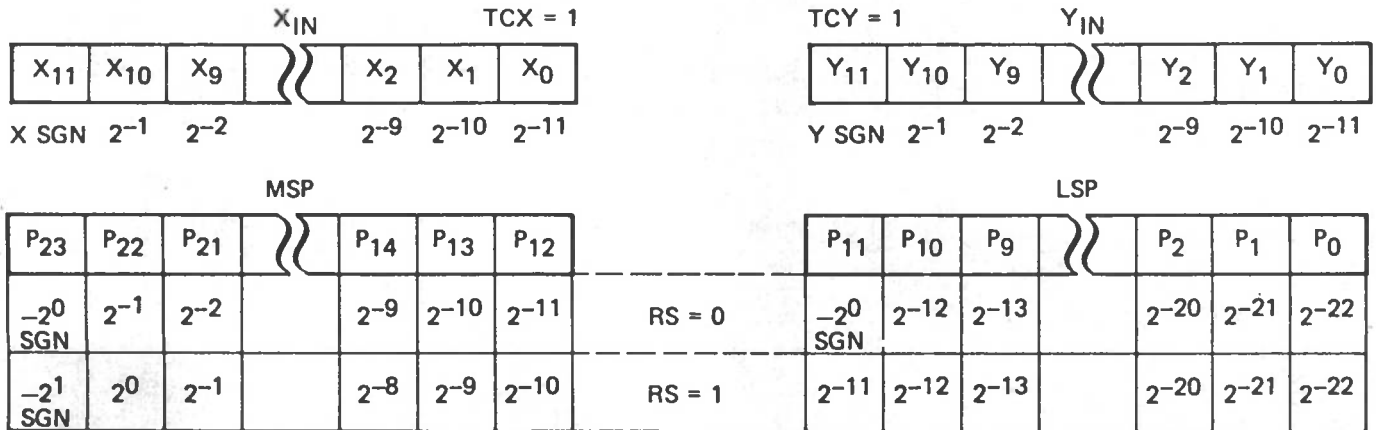
Electrical and switching characteristics over V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	DEVICE	TYP*	COMMERCIAL	MILITARY	UNIT
Clocked multiply time τ_{mc}	See Figure 6	MPY-12	80	110	140	nsec
		MPY-16	100	140	185	nsec
Unclocked multiply time, τ_{muc}	See Figure 6	MPY-12	105	145	180	nsec
		MPY-16	125	175	225	nsec
I_{CC} supply current		MPY-12 see Figure 12	400	540	600	mA
		MPY-16 see Figure 13	600	800	900	mA

*NOTE: At $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$

INPUT/OUTPUT FORMATS

FRACTIONAL TWO'S COMPLEMENT



$$X = -1 * X_{SIGN} + \sum_{n=1}^{11} X_n 2^{-n}$$

$$P = -1 * P_{SIGN} + \sum_{n=1}^{22} P_n 2^{-n}$$

The resulting values for X and P given in the above evaluations (Y is expressed in the same manner as X) are in fractional two's complement format. The value for the sign variable is 0 for positive or zero numbers and 1 for negative numbers.

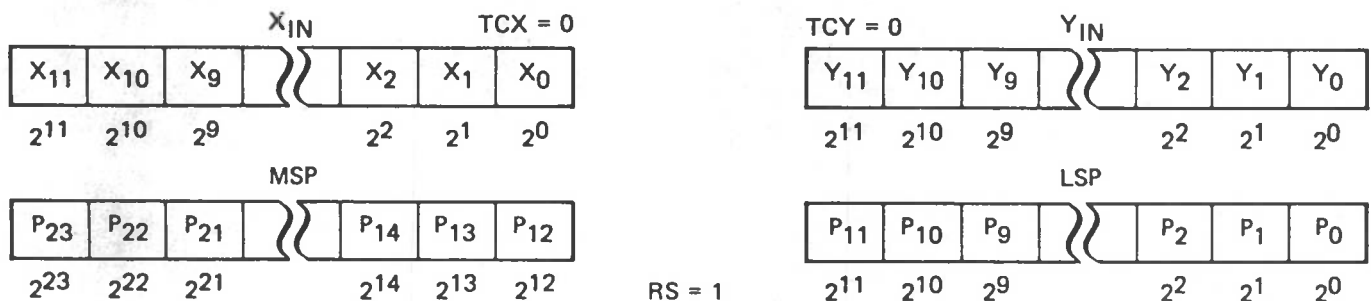
RS = 0 An overflow occurs in the attempted multiplication of the two's complement number 1.0000 . . . (-1 base 10) with itself, yielding a result of the same number, i.e.,

$$(-1)_{10} * (-1)_{10} = (-1)_{10}$$

The product sign bit is available redundantly as the MSB of both the MSP and LSP words.

RS = 1 No overflow occurs when multiplying $-1_{(10)}$ times $-1_{(10)}$. The product is a true $+1.0_{(10)}$; i.e., product bit P_{22} is a 1, all other bits are 0.

INTEGER MAGNITUDE

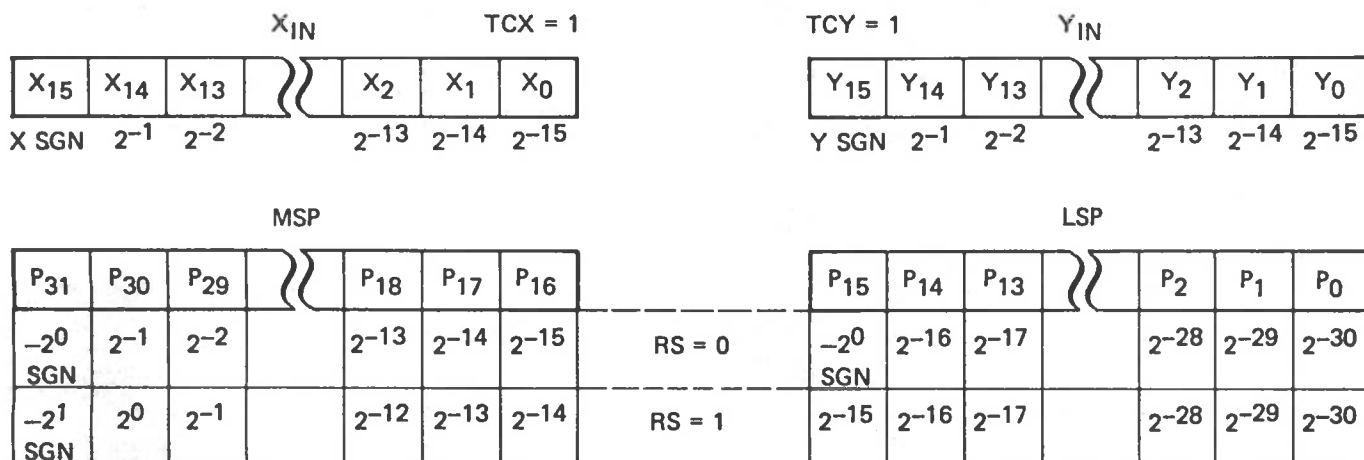


Note: (1) When doing unsigned magnitude or mixed mode multiplications, RS must be a 1 to get a valid product.

(2) When doing mixed mode (two's complement times unsigned magnitude) multiplies, P_{23} is the product sign bit.

INPUT/OUTPUT FORMATS

FRACTIONAL TWO'S COMPLEMENT



$$X = -1 * X_{SIGN} + \sum_{n=1}^{15} X_n 2^{-n}$$

$$P = -1 * P_{SIGN} + \sum_{n=1}^{30} P_n 2^{-n}$$

The resulting values for X and P given in the above evaluations (Y is expressed in the same manner as X) are in fractional two's complement format. The value for the sign variable is 0 for the positive or zero numbers and 1 for negative numbers.

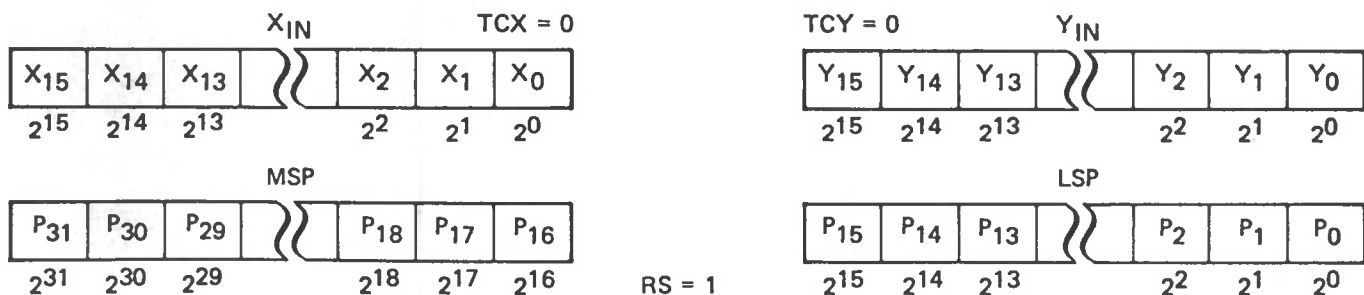
RS = 0 An overflow occurs in the attempted multiplication of the two's complement number $1.0000 \dots (-1 \text{ base } 10)$ with itself, yielding a result of the same number, i.e.,

$$(-1)_{10} * (-1)_{10} = (-1)_{10}$$

The product sign bit is available redundantly as the MSB of both the MSP and LSP words.

RS = 1 No overflow occurs when multiplying $-1_{(10)}$ times $-1_{(10)}$. The product is a true $+1.0_{(10)}$; i.e., product bit P_{30} is a 1, all other bits are 0.

INTEGER MAGNITUDE



- Note:
- (1) When doing unsigned magnitude or mixed mode multiplications, RS must be a 1 to get a valid product.
 - (2) When doing mixed mode (two's complement times unsigned magnitude) multiplies, P_{31} is the product sign bit.

MPY-24HJ

24 X 24 BIT PARALLEL MULTIPLIER

The MPY-24HJ is a high-speed TTL LSI device. It is a 24 x 24-bit parallel two's complement or magnitude multiplier with a double precision output. Its low power and high performance are the result of circuits developed and patented by TRW. The multiplier array logic achieves a speed-power performance of less than 1 picojoule per gate.

Three registers are used in the MPY-24HJ multiplier. The two 24 bit input registers are positive edge triggered, and have independent clocks. The 48 bit output register is a level-dependent latch. As such, the outputs can be used either synchronously or asynchronously (transparent).

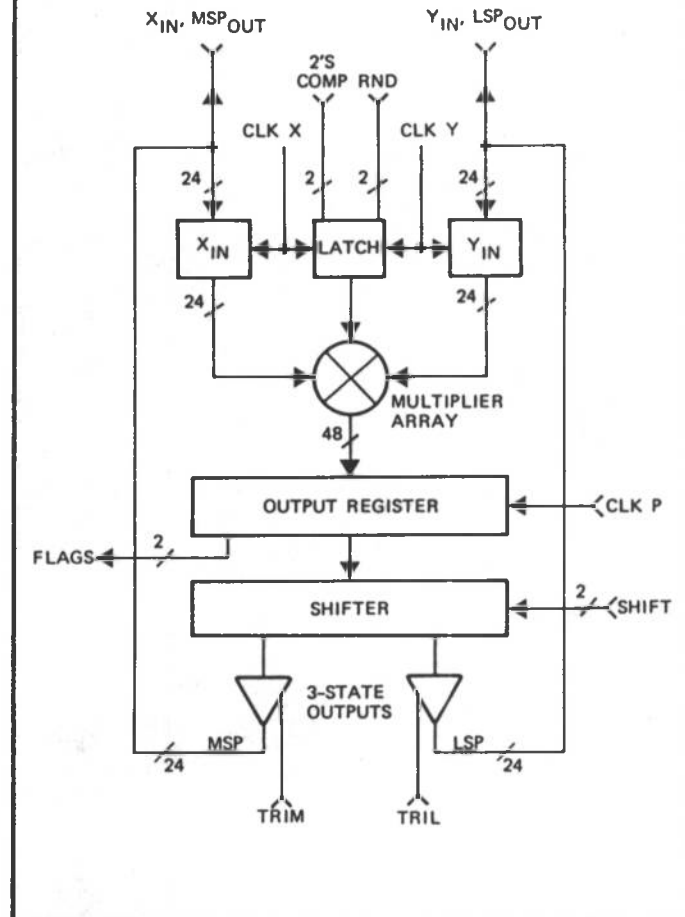
Applications for the MPY-24HJ include high speed, high accuracy digital signal processing, digital filters, and the fast Fourier transform. It is particularly suited to doing the mantissa multiply in floating point multiplication.

The modular architecture of the MPY-24HJ allows straightforward implementation of larger array multipliers such as 48 x 48 bits.

FEATURES

- 24 x 24 bit parallel multiply
- Single chip bipolar technology
- Two's complement or magnitude (can be mixed)
- 200 nsec synchronous multiply
- 225 nsec asynchronous multiply (output register transparent)
- Includes input and output registers
- Much lower power than MSI equivalent multipliers
- Radiation-hard
- Three-state outputs
- Uniform rounding available
- Overflow and normal flags for floating point multiply
- Built-in shifter for floating point normalization or scaling
- TTL inputs and outputs
- Single power supply, +5V

MPY-24HJ LOGIC BLOCK DIAGRAM



CONTROLS

(Positive logic unless otherwise noted)

CLK X — X_{IN} Register Clock

CLK Y — Y_{IN} Register Clock

CLK P — Output Register Clock

TRIL — LSP Three-State Control

TRIM — MSP Three-State Control

SH A, SH B — Shifts the output product zero, one or two bits upward, adds trailing zeros

OVF — Flags the two's complement output as overflowed (see figure 18)

NORM — Flags the two's complement output as already normalized (see figure 18)

RND A, RND B — Adds 1 to one of 3 places

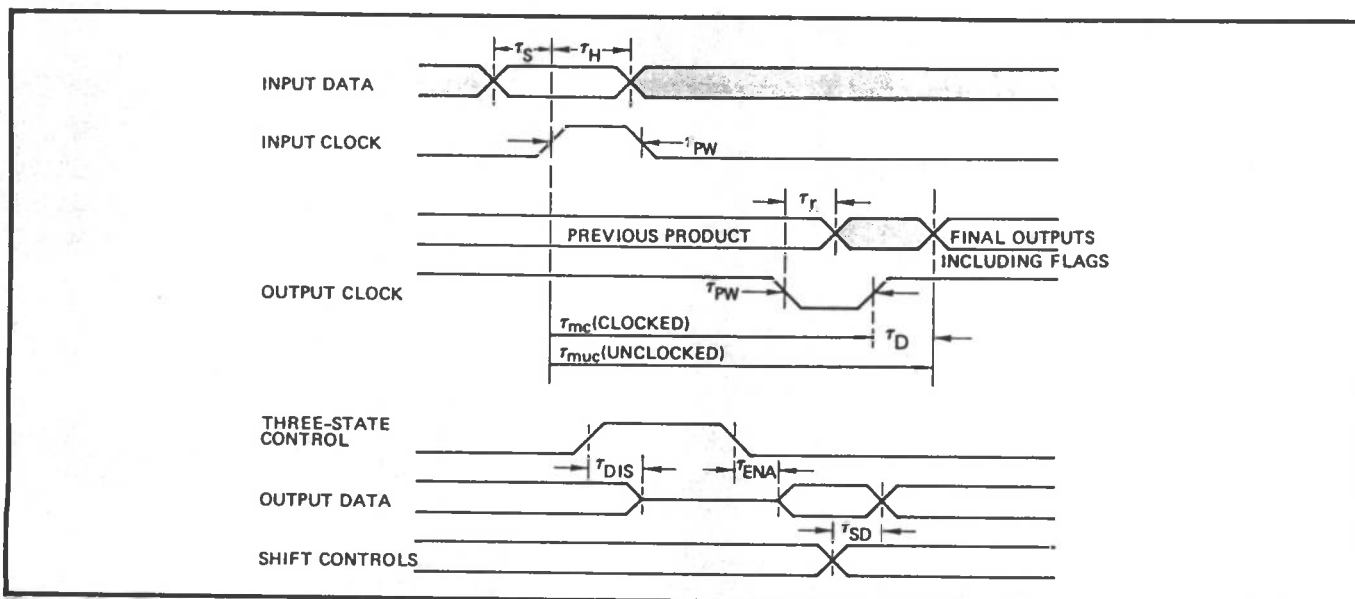


Figure 14. Timing Diagram

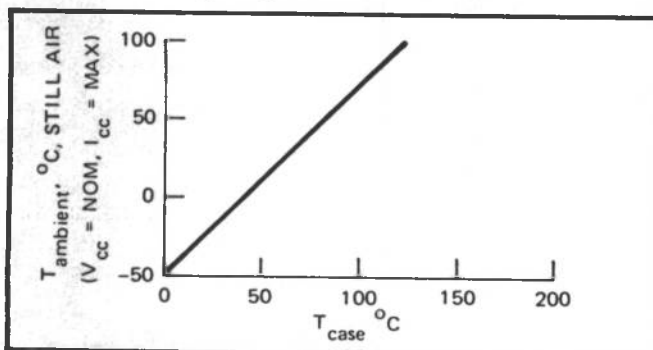
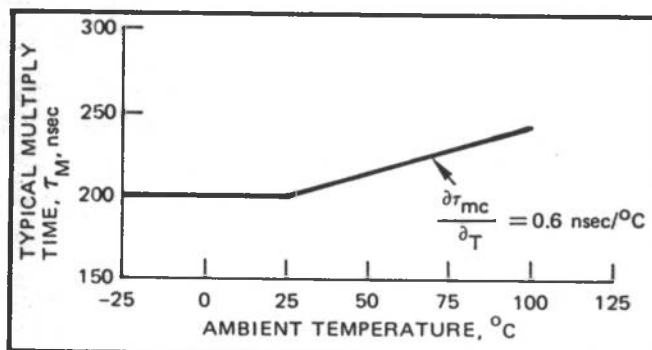
Figure 15. T_{ambient} Versus T_{case} 

Figure 16. Clocked Multiply Time Versus Temperature

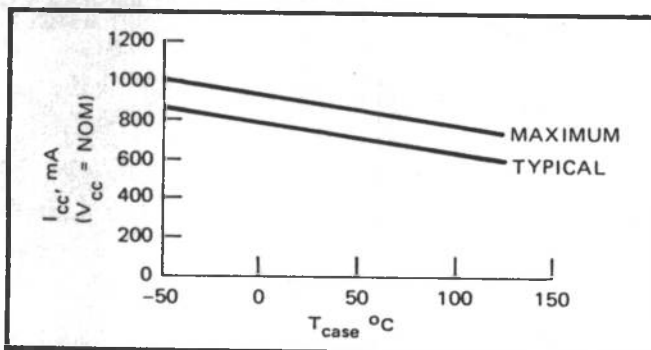
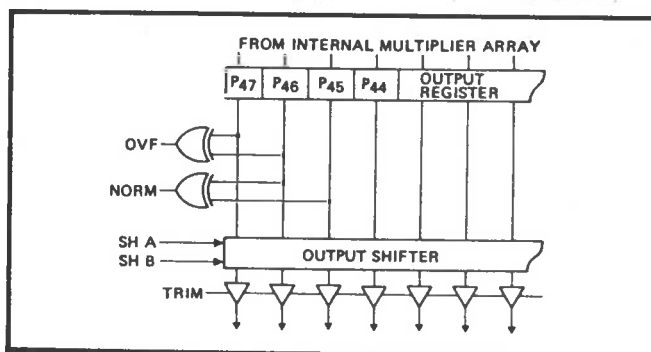
Figure 17. I_{CC} Versus T_{case} 

Figure 18. Output Detail

Electrical and switching characteristics over V_{CC} and temperature ranges (except as otherwise noted)

PARAMETER	TEST CONDITIONS	TYP*	MAX		UNIT
			COMMERCIAL	MILITARY	
Clocked multiply time, τ_{mc}	See Figure 14	200	285	320	nsec
Unclocked multiply time, τ_{muc}	See Figure 14	225	325	365	nsec
Shift delay, τ_{SD}	See Figure 14	25	35	40	nsec
CLK P release time, τ_r	See Figure 14	25	35	40	nsec
Supply current, I_{CC}	See Figure 17	700	850	1000	mA

*Note: at $V_{\text{CC}} = 5.0 \text{ V}$, $T_A = 25^\circ\text{C}$

CONTROL AND CLOCK TRUTH TABLE AND LOGIC DESCRIPTION

All inputs, outputs, and controls are TTL compatible; positive logic

CONTROL MNEMONIC	LOGIC STATE	FUNCTION
Data Input/Output		Positive logic, Logic 1 = $1 * 2^n$
CLK X, CLK Y		Loads internal X_{IN} , Y_{IN} register on 0 to 1 transition. Holds data until next 0 to 1 transition. D type register.
CLK P	$\uparrow$ 1 $\downarrow$ 0	Freezes internal output latches on 0 to 1 transition. Holds last latched state. Releases latched state to follow mode on 1 to 0 transition. Unclocked mode. Output register continuously follows the array product.
TCX (Mode Control, X input) TCY (Mode Control, Y input)	1 0	Registered controls clocked by (CLK X or CLK Y). Two's complement number system. Unsigned magnitude number system (for expandable case, see text and diagrams)
OVF	0 1	Signals P_{47} and P_{46} are of the same state. Signals P_{47} and P_{46} are opposite states.
NORM	0,1	Same as flag overflow for P_{46} and P_{45} .
SH B	SH A	Direct nonregistered inputs, no effect on flag outputs.
0	0	No shift, MSP bit has weight of $1 * 2^{47}$ magnitude notation.
0	1	Shift up one bit, MSP has weight of $1 * 2^{46}$, $P_0 = 0$.
1	X	Shift up two bits, MSP has weight of $1 * 2^{45}$, $P_0, P_1 = 0$.
RND B	RND A	Registered controls clocked by (CLK X or CLK Y).
0	0	<u>Two's Complement</u> No round.
0	1	Adds $1 * 2^{-25}$ to product.
1	0	Adds $1 * 2^{-24}$ to product.
1	1	Adds $1 * 2^{-23}$ to product.
		<u>Magnitude</u> No round.
		Adds $1 * 2^{21}$ to product.
		Adds $1 * 2^{22}$ to product.
		Adds $1 * 2^{23}$ to product.
TRIL, TRIM	0 1	Three-state controls on outputs. TRIL operates on LSP, TRIM on MSP. Output enabled, output is low impedance. Output disabled, output is high impedance.

TYPICAL OPERATING SEQUENCE (TWO PORT) FOR REPEATED SETS OF MULTIPLICATIONS

- 1) Load 24 bit multiplier (N_0) and 24 bit multiplicand (M_0) into X and Y input registers. Simultaneously load output registers with the product of two previous operands, N_{-1} and M_{-1} . Three-state controls are in high state.
- 2) During the multiplication period of $N_0 * M_0$, the previous product $N_{-1} * M_{-1}$ is read to the I/O bus by placing the three-state controls in the low state. Following the product read period, the three-state controls are again returned to the high state and new operands N_1 and M_1 are sourced to the bus. The procedure is repeated by returning to item 1 above. In this way, a continual pipelined multiplication set is performed each τ_m period. Timing diagrams are shown below.

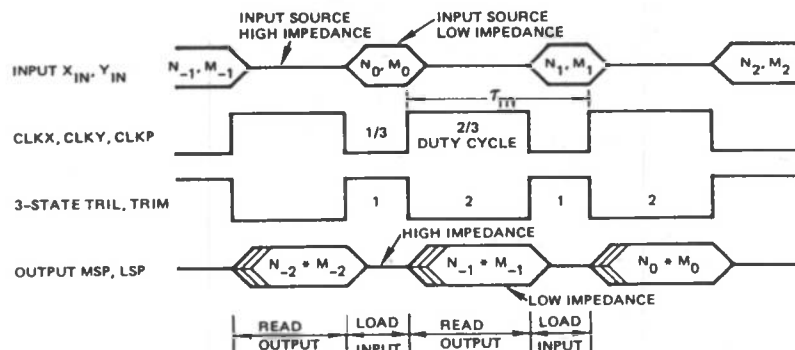
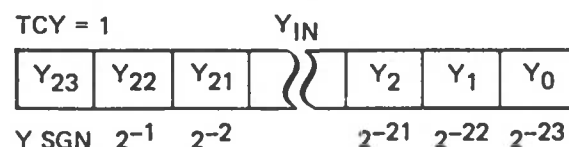
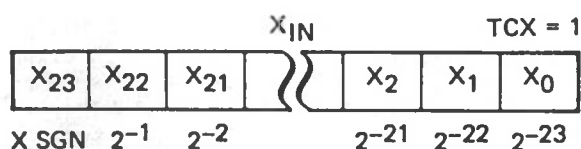


Figure 19. Multiplexed I/O Timing Diagram

DATA FORMAT EXAMPLES

FRACTIONAL TWO'S COMPLEMENT



MSP _{OUT}								LSP _{OUT}						
P ₄₇	P ₄₆	P ₄₅		P ₂₆	P ₂₅	P ₂₄		P ₂₃	P ₂₂	P ₂₁		P ₂	P ₁	P ₀
-2 ¹	2 ⁰	2 ⁻¹		2 ⁻²⁰	2 ⁻²¹	2 ⁻²²	SH A = SH B = 0	2 ⁻²³	2 ⁻²⁴	2 ⁻²⁵		2 ⁻⁴⁴	2 ⁻⁴⁵	2 ⁻⁴⁶
P SGN														
2 ⁰	2 ⁻¹	2 ⁻²		2 ⁻²¹	2 ⁻²²	2 ⁻²³	SH A = 1 SH B = 0	2 ⁻²⁴	2 ⁻²⁵	2 ⁻²⁶		2 ⁻⁴⁵	2 ⁻⁴⁶	0
2 ⁻¹	2 ⁻²	2 ⁻³		2 ⁻²²	2 ⁻²³	2 ⁻²⁴	SH A = X SH B = 1	2 ⁻²⁵	2 ⁻²⁶	2 ⁻²⁷		2 ⁻⁴⁶	0	0

Note: In all multiply cases except -1.0(10) X -1.0(10), the two MSB bits (-2¹ and 2⁰) are the same. In that one multiply case, -2¹ will be a 0 and 2⁰ will be a 1, all other bits will be 0. The OVF flag (-2¹ ⊕ 2⁰) will be a 1, and the NORM flag (2⁰ ⊕ 2⁻¹) will also be a 1. Since these flags are generated before the output shifter, the shift position will have no effect on the states of the flags. See figure 18.

Fractional 2's complement

$$X = -1 * \text{SGN} + \sum_{n=1}^{23} X_n 2^{-n}$$

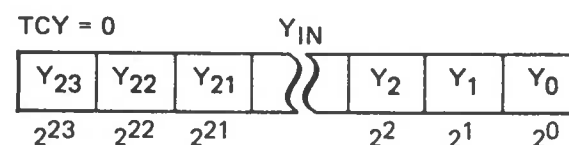
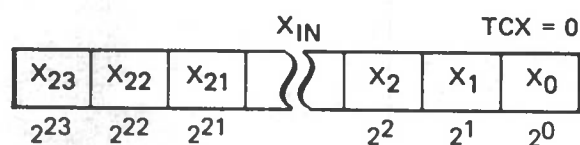
$$P = -1 * \text{PSGN} + \sum_{n=0}^{46} P_n 2^{-n}$$

Magnitude

$$X = \sum_{n=0}^{23} X_n 2^n$$

$$P = \sum_{n=0}^{47} P_n 2^n$$

INTEGER MAGNITUDE



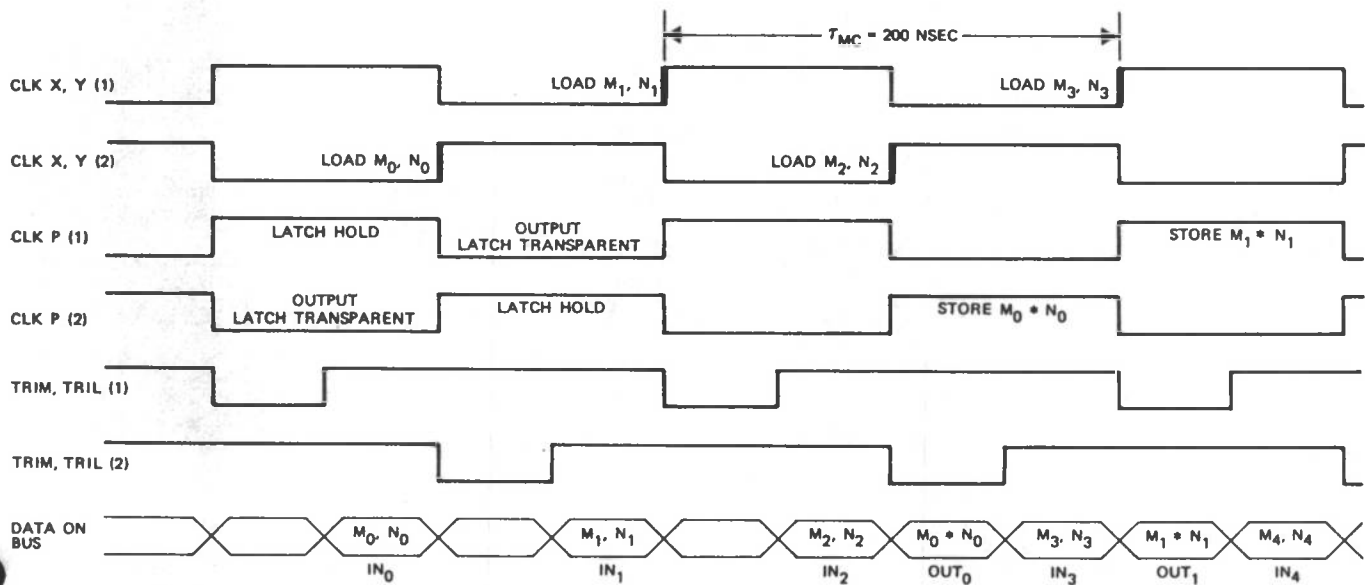
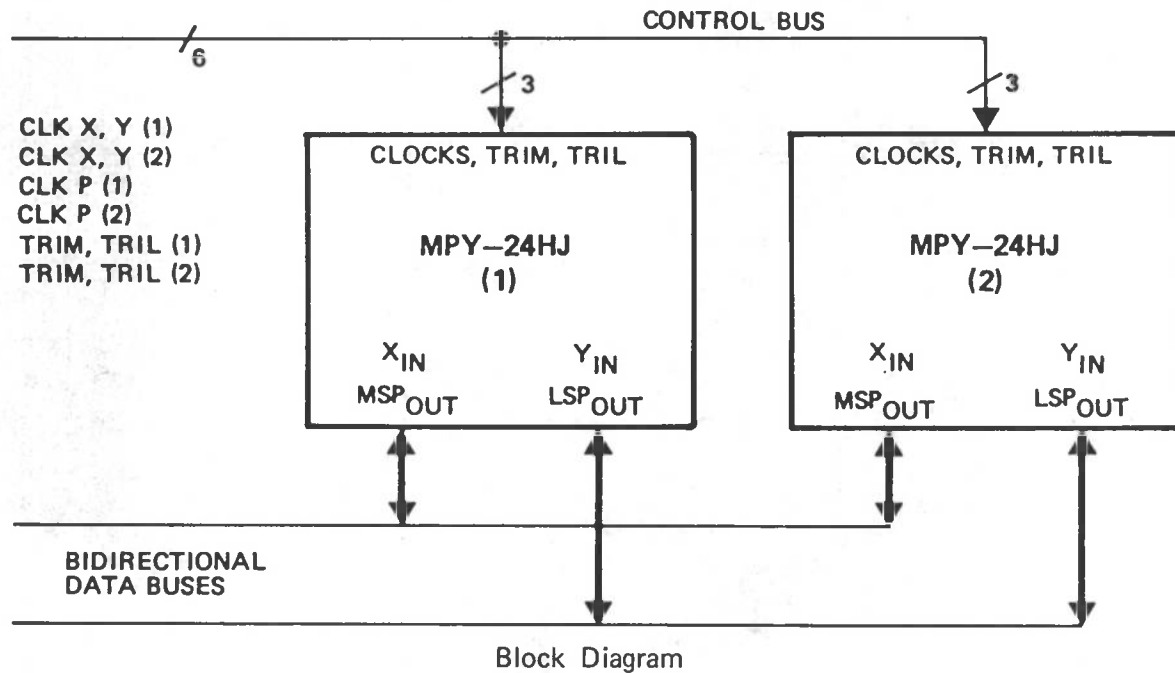
MSP _{OUT}								LSP _{OUT}						
P ₄₇	P ₄₆	P ₄₅		P ₂₆	P ₂₅	P ₂₄		P ₂₃	P ₂₂	P ₂₁		P ₂	P ₁	P ₀
2 ⁴⁷	2 ⁴⁶	2 ⁴⁵		2 ²⁶	2 ²⁵	2 ²⁴	SH A = SH B = 0	2 ²³	2 ²²	2 ²¹		2 ²	2 ¹	2 ⁰
2 ⁴⁶	2 ⁴⁵	2 ⁴⁴		2 ²⁵	2 ²⁴	2 ²³	SH A = 1 SH B = 0	2 ²²	2 ²¹	2 ²⁰		2 ¹	2 ⁰	0
2 ⁴⁵	2 ⁴⁴	2 ⁴³		2 ²⁴	2 ²³	2 ²²	SH A = X SH B = 1	2 ²¹	2 ²⁰	2 ¹⁹		2 ⁰	0	0

When mixed mode signals are used, the flag signals, FLAG OVFL0 and FLAG NORM will not have the same general utility as described under FLAG outputs.

APPLICATION NOTES

100 NSEC 24 X 24 BIT MULTIPLIER

The multipliers can be interfaced easily on a data bus (or buses) to achieve greater multiply throughput rates. The MPY-24HJ was picked for the example below because it has the highest number of multiplexed I/O ports. The MPY-12HJ and MPY-16HJ (single precision mode), with their individual inputs and outputs, are easier to interface because the buses do not have to be multiplexed for a given throughput rate. The timing for the clocks and three-state controls of this circuit are given below.

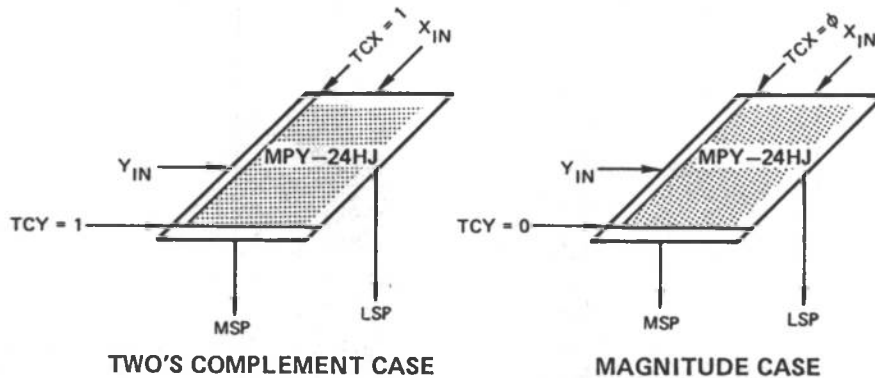


APPLICATION NOTES

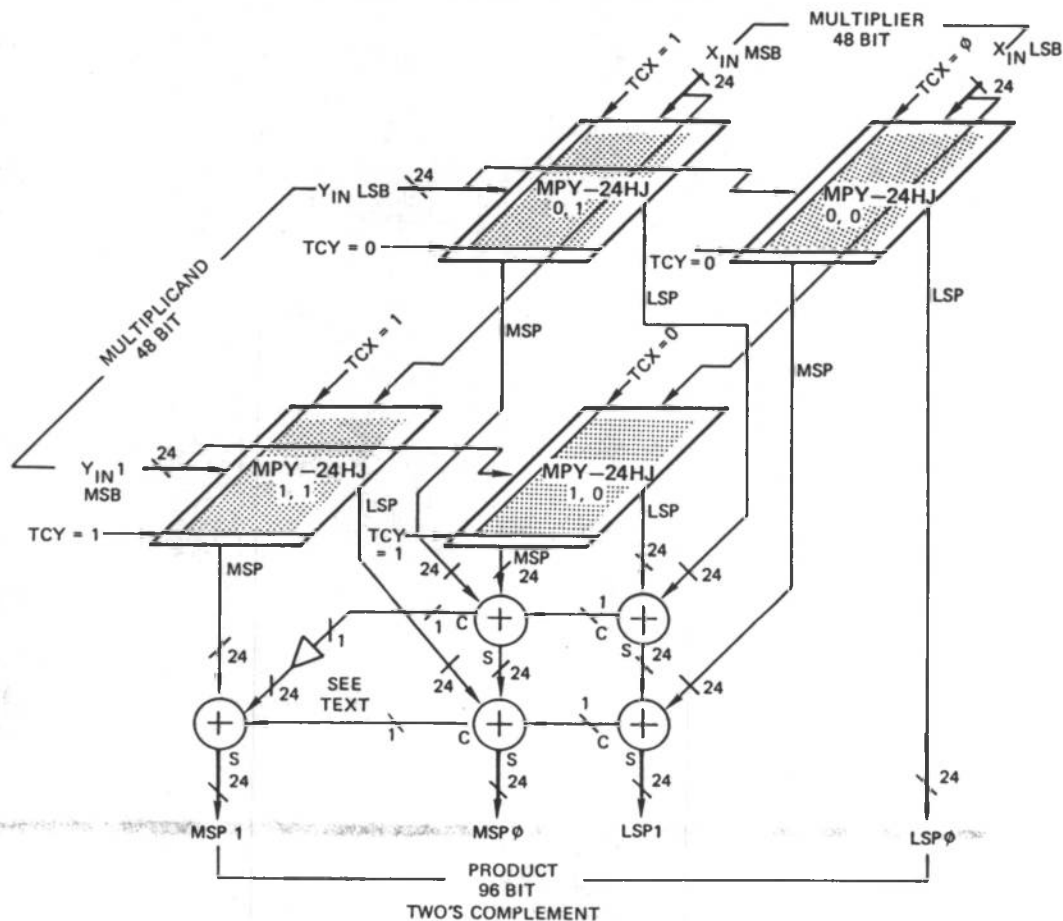
48 X 48 TWO'S COMPLEMENT MULTIPLIER

The expanded two's complement diagram shows the connections to external adders required to complete the partial product summation. The diagram simplified for illustrative purposes is accurate, but for speed optimization additional registers can be used to pipeline the additions. Each adder shown is a 24 bit wide two input adder or equivalent. Carry-in and carry-out are also required.

The expanded magnitude case is similar except all TC controls are set low, logic 0, and the upper carry into the last most significant adder connects only to the least significant bit of the adder. The remaining 23 inputs to the adder are then terminated to logic zero, ground.



TWO'S COMPLEMENT MULTIPLIER, MULTIPLICAND



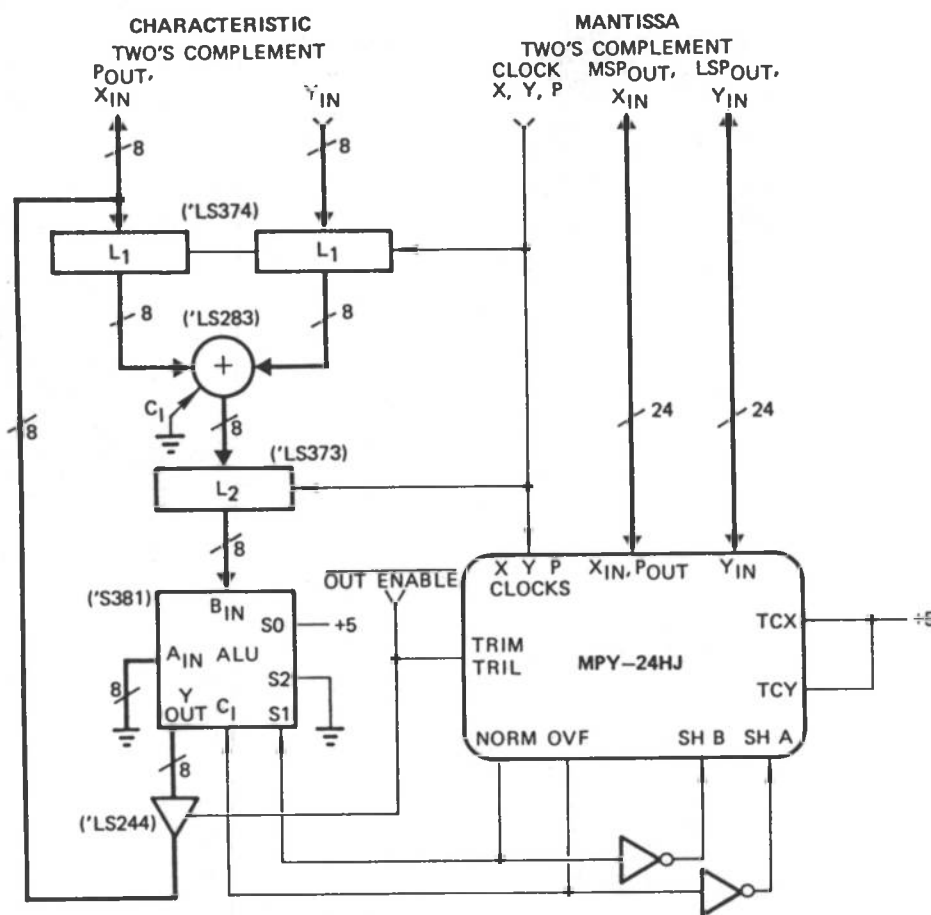
APPLICATION NOTES

32 BIT FLOATING POINT MULTIPLICATION—TWO'S COMPLEMENT

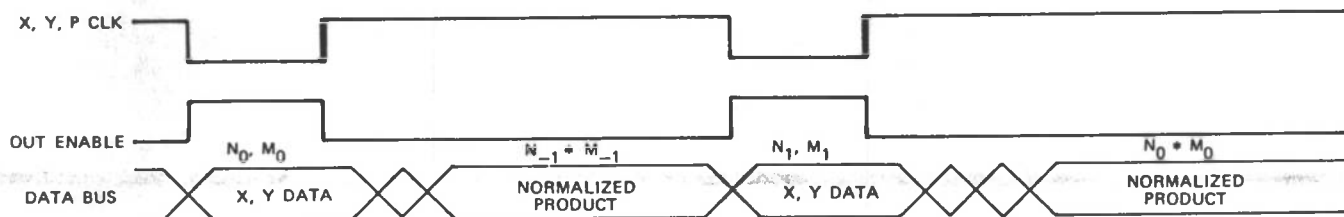
The MPY-24HJ, with its shifter, is ideally suited for floating point multiplication applications. The most complex part of the function, the mantissa multiply plus normalize, can now be done with 1 chip. The cost, power, and size of the floating point multiply function can be greatly reduced. The latches and adders shown are chosen to closely match the setup, hold, and output delay times of the MPY-24HJ. Split timing is used to read the products and load new operands via common buses.

The multiply time is divided into two phases defined by the clock. At the rising edge of the X, Y, P clock, a new multiplier and multiplicand are stored in the input latches of the MPY-24HJ and L₁ latches. While the internal multiplier array of the MPY-24HJ is generating a product, the two characteristics are added. When the clock goes low and then high again, the product is stored in the output latch of the MPY-24HJ, and L₂ (new operands could also be read in again). The flag outputs of the multiplier chip are then used to normalize the characteristic and mantissa of the product. Although not shown here, many floating point users test for an overflow of the characteristic after final normalization, setting a flag or hard limiting if it does.

When the output shifter and ALU have settled, the normalized product is put onto the bus and read back.



Two's Complement Block Diagram

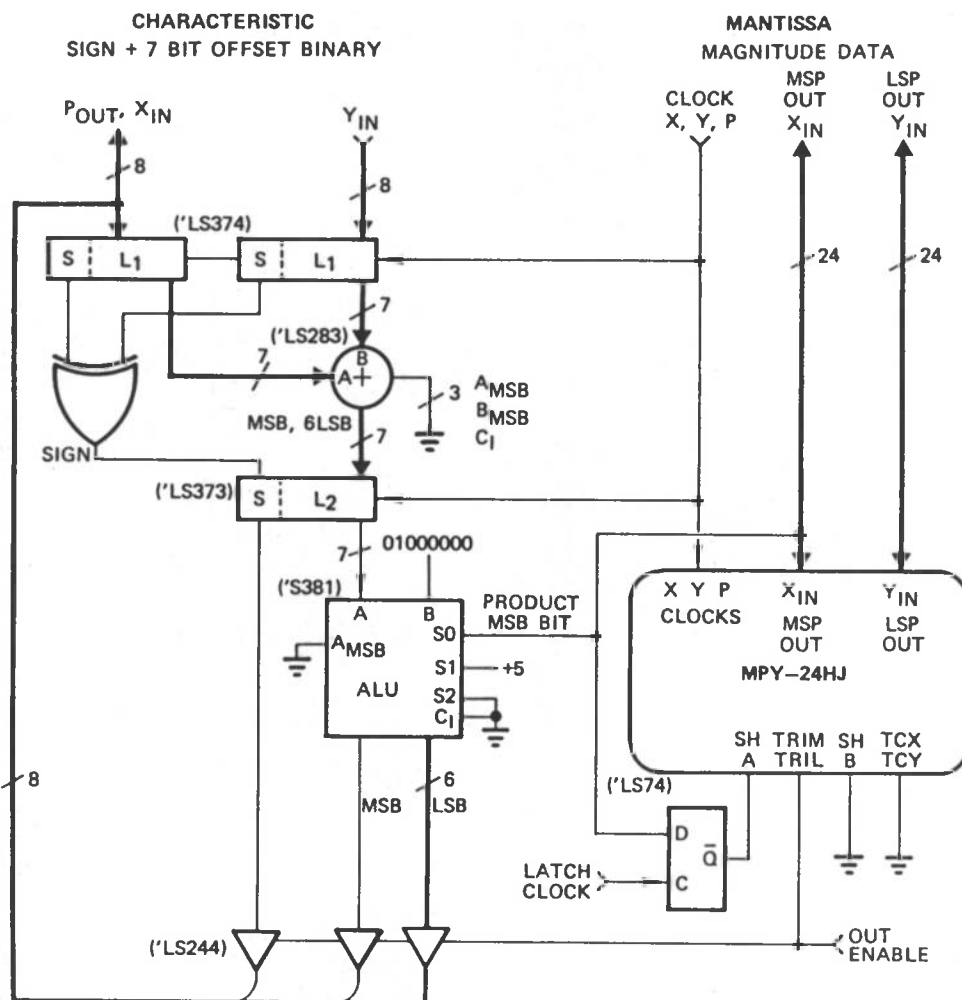


Two's Complement I/O Timing Diagram

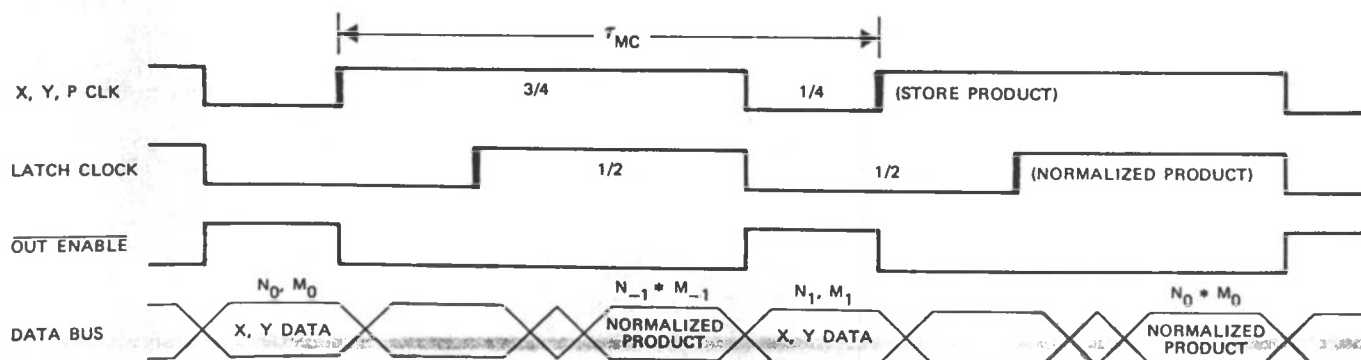
APPLICATION NOTES

32 BIT FLOATING POINT MULTIPLICATION—MAGNITUDE

The basic multiply time is partitioned into three phases defined by the clocks. At the rising edge of the X, Y, P clock, new X and Y operands are loaded into the input latches. Simultaneously, the previous product is stored in the output registers of the MPY-24HJ and 'LS373. The MSB of the mantissa is read into the ALU to adjust the exponent, and also into the 'LS74 latch where it is stored on the rising edge of the latch clock. Shortly after that edge, the MPY-24HJ output will be normalized and may be read, along with the output of the ALU. When the output enable goes high, the output buffers are turned off. New X and Y operands can now be brought in prior to the next X, Y, P clock.



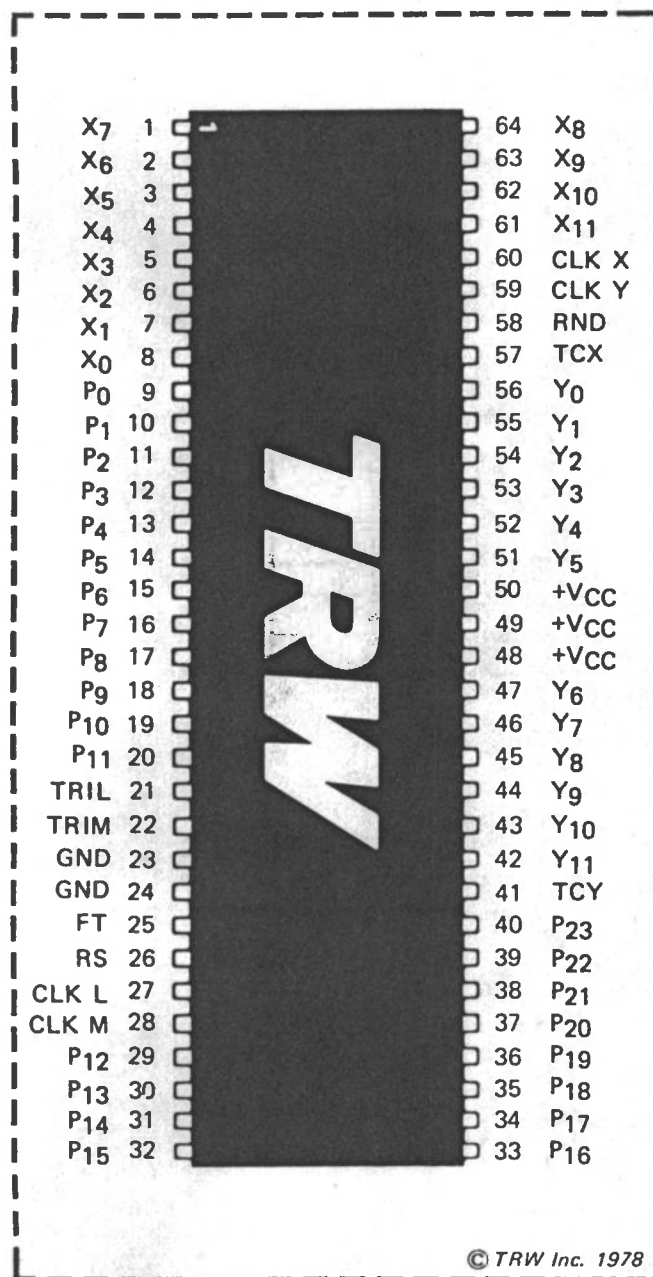
32 Bit Floating Point Multiplier Block Diagram



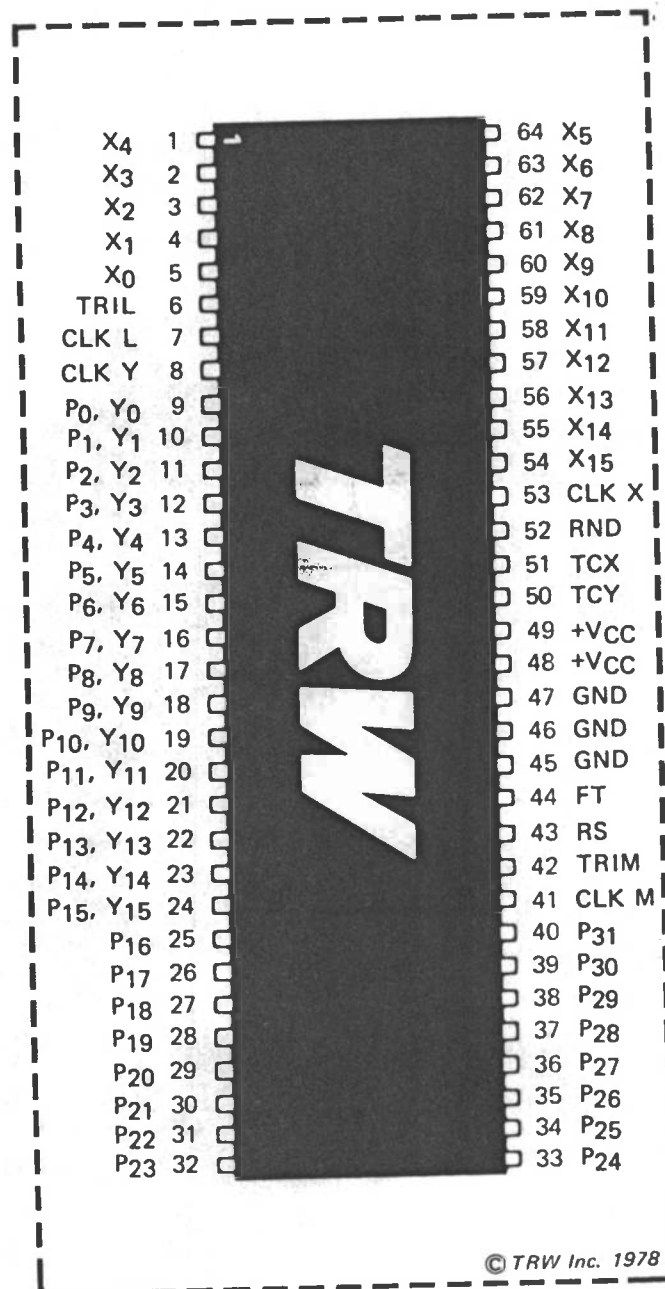
Magnitude I/O Timing Diagram

PACKAGE INFORMATION

MPY-12HJ



MPY-16HJ

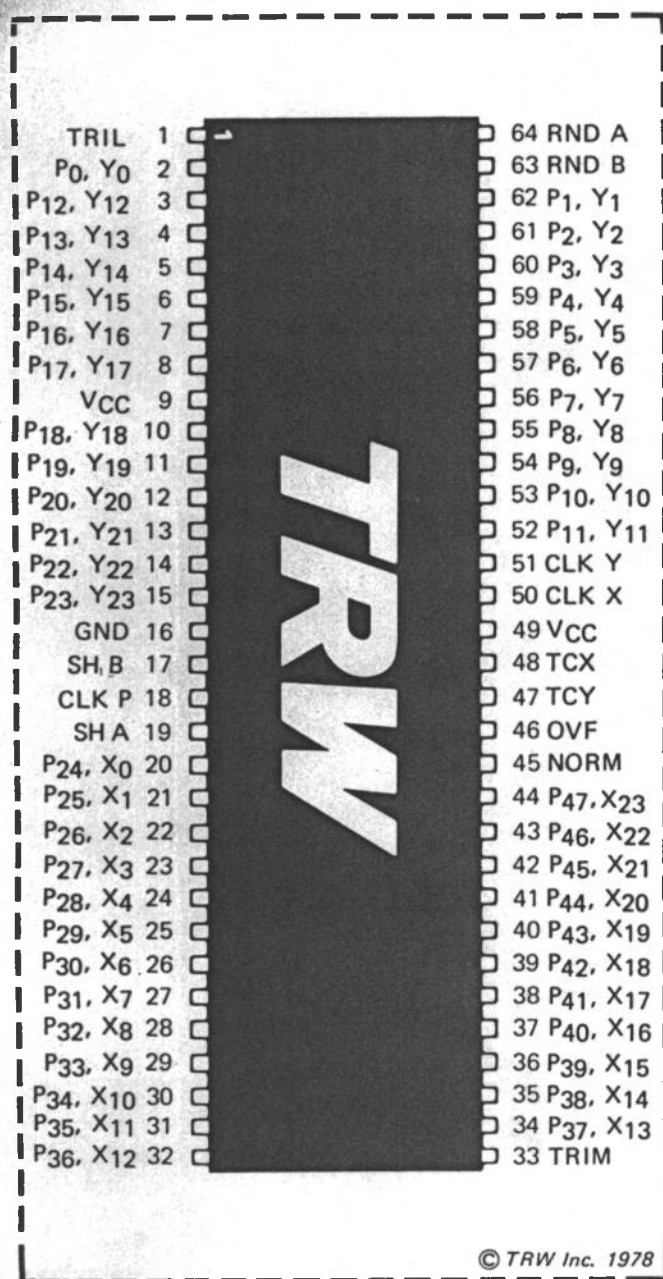


FRACTIONAL/INTEGER MULTIPLICATION

The MPY-series multipliers may be used in either a fractional or integer mode — the difference is conceptual. For example, using a 4-bit case, the multiplier does not know (or care) whether it is performing the multiplication $6 \times (-2) = -12$ or $(6/8) \times (-2/8) = -12/64$; the input and output binary fields will be the same. Fractional multiplication (using fields as defined in the previous specifications) offers the advantage of more convenient single precision usage. The MSB is closest to the binary point in fractional representation (the LSB for integer representation). The fractional notation is frequently the most convenient when implementing a floating point multiplication system.

PACKAGE INFORMATION

MPY-24HJ

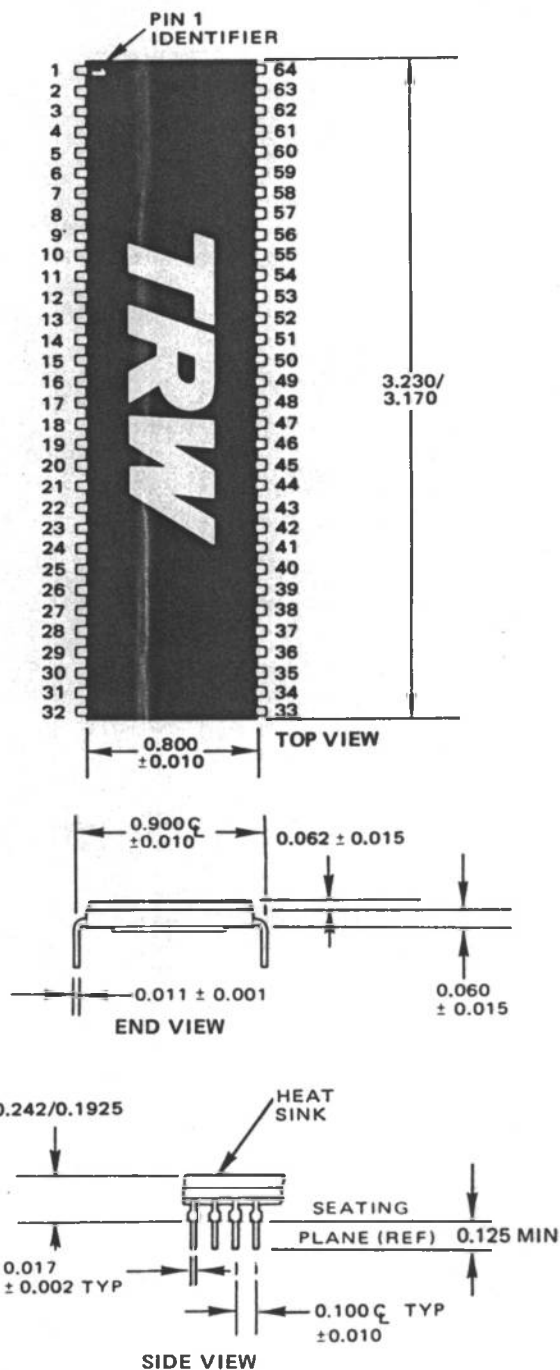


THERMAL RESISTANCE DATA

Junction to case $\theta_{JC} \approx 4^{\circ}\text{C/W}$ Case to ambient θ_{CA} (Still air) $\approx 10^{\circ}\text{C/W}$ Case to ambient θ_{CA} (300 cfm airflow) $\approx 4^{\circ}\text{C/W}$

TRW RESERVES THE RIGHT TO CHANGE PRODUCTS AND SPECIFICATIONS WITHOUT NOTICE. THIS INFORMATION DOES NOT CONVEY ANY LICENSE UNDER PATENT RIGHTS OF TRW INC. OR OTHERS.

64-PIN DIP



NOTES

- DIMENSIONS IN INCHES
- ALL POWER AND GROUND PINS MUST BE CONNECTED

TRW SALES OFFICES

ALABAMA, Huntsville	(205) 533-7600	NEBRASKA, Lincoln	(402) 474-5151
ARIZONA, Phoenix	(602) 971-6250	NEW MEXICO, Albuquerque	(505) 265-7759
CALIFORNIA, Los Angeles	(213) 478-0183	NEW YORK, Rochester	(716) 424-2830
Mountain View	(415) 969-6060	NORTH CAROLINA, Charlotte	(704) 527-1344
San Diego	(714) 571-1544	OHIO, Cincinnati	(513) 521-2290
Tustin	(714) 832-4952	Columbus	(614) 888-9396
COLORADO, Westminster	(303) 426-0890	Dayton	(513) 298-9546
CONNECTICUT, Orange	(203) 795-3515	Middleburg Heights	(216) 826-4424
Rowayton	(203) 853-4466	OREGON, Beaverton	(503) 643-1644
FLORIDA, Ft. Lauderdale	(305) 721-1700	PENNSYLVANIA, Bala Cynwyd	(215) 667-3400
Orlando	(305) 857-3650	Pittsburgh	(412) 344-7277
ILLINOIS, Elk Grove Village	(312) 593-0200	TENNESSEE, Greeneville	(615) 639-6154
INDIANA, Fort Wayne	(219) 432-5591	TEXAS, Austin	(512) 451-2959
Indianapolis	(317) 359-9283	Dallas	(214) 387-3030
Kokomo	(317) 453-3592	Houston	(713) 772-5541
IOWA, Cedar Rapids	(319) 393-8703	UTAH, Salt Lake City	(801) 943-5650
KANSAS, Prairie Village	(913) 236-4646	VIRGINIA, Richmond	(804) 288-8334
Wichita	(316) 686-6685	WASHINGTON, Bellevue	(206) 454-0300
KENTUCKY, Louisville	(502) 897-1569	WISCONSIN, Wauwatosa	(414) 475-7755
MARYLAND, Baltimore	(301) 795-5775	CANADA	
MASSACHUSETTS, Waltham	(617) 890-3232	BRITISH COLUMBIA, Vancouver	(604) 874-2422
MICHIGAN, Grand Rapids	(616) 942-5420	MANITOBA, Winnipeg	(204) 775-3354
Southfield	(313) 559-5454	ONTARIO, Toronto	(416) 494-5445
St. Joseph	(616) 983-7337	QUEBEC, Montreal	(514) 341-6420
MINNESOTA, Minneapolis	(612) 854-4600		
MISSOURI, St. Louis	(314) 432-2830		

INTERNATIONAL SALES OFFICES

ARGENTINA, Buenos Aires	404122	JAPAN, Tokyo	4615121
AUSTRALIA, Kingsgrove N.S.W.	500111	NETHERLANDS, Amsterdam	934824
AUSTRIA (see Germany)		NEW ZEALAND, Wellington	51279
BELGIUM, Brussels	6600012	NORWAY, Oslo	553893
BRAZIL, Sao Paulo	2409211	SOUTH AFRICA, Capetown	457656
DENMARK, Herlev	842000	Johannesburg	6181027
FINLAND, Helsinki	601155	SPAIN, Madrid	2425204
FRANCE, Paris	7581111	SWEDEN, Vallingby, Stockholm	248340
GERMANY, Munich	7146065	SWITZERLAND, Zurich	429900
ISRAEL, Tel Aviv	444572	TAIWAN, Taipei	7512062
ITALY, Monza	360021	UNITED KINGDOM, London	9025941

TRW LSI PRODUCTS

P.O. BOX 1125, REDONDO BEACH, CALIFORNIA 90278
(213) 535-1831

Model: MPY-8HUI

PRELIMINARY INFORMATION

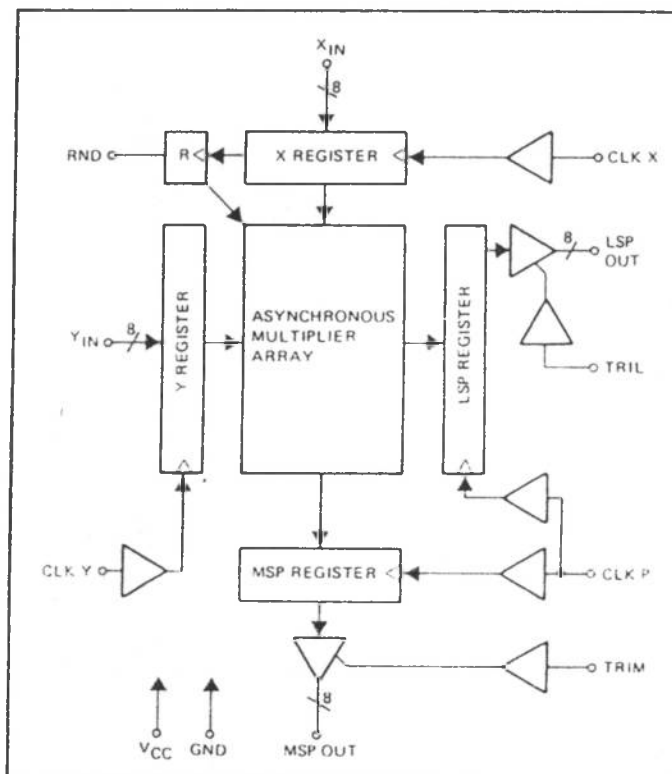
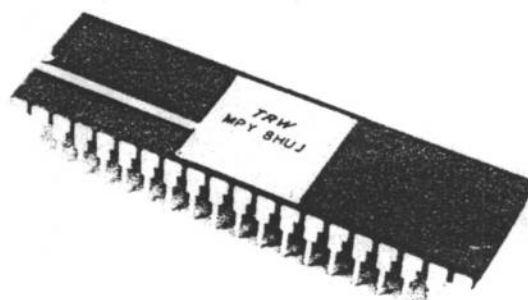
The MPY-8HUI is a high speed, TTL LSI 8 x 8 bit parallel array multiplier, operating on unsigned magnitude inputs, and yielding a double precision product. Its low power and high performance is the result of a proven method developed and patented by TRW (U.S. Patent No. 3,900,724). The main internal multiplier array logic achieves a speed-power performance of less than 0.8 pico-joules per equivalent gate.

Four input and output registers are provided, along with 3-state outputs. These registers are positive-edge triggered D-type flip-flops with independent clocks.

Applications for the MPY-8HUI include digital video signal processing and digital filtering. It is ideal for extending the multiplication capabilities of microcomputers, since all the interface circuitry but the address and clock decoder is included on chip (see page 6). This multiplier is pin-compatible to the MPY8HJ and MPY8AJ, except that it operates on unsigned magnitude numbers, while they operate on two's complement numbers.

FEATURES

- Double precision product
- 45 nanosecond typical multiply time
- Much lower power/less space than MSI equivalent multipliers
- Includes input and output registers
- Single chip, bipolar, TTL
- Single bus or multiport operation
- Radiation hard
- Three-state outputs
- Single power supply, +5V
- Easy interface to microprocessors
- Zero-nanosecond register hold time
- Worst case specs across full voltage and temperature ranges



MPY-8HUU

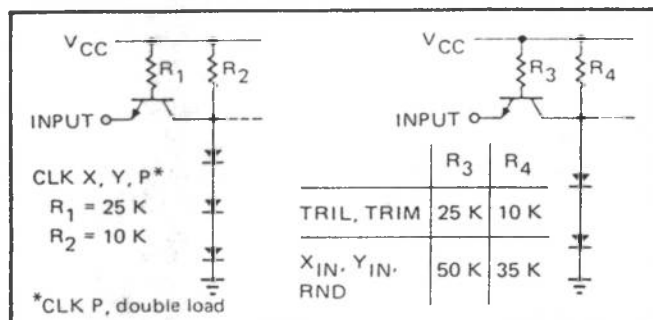


Figure 1. Equivalent Input Schematics

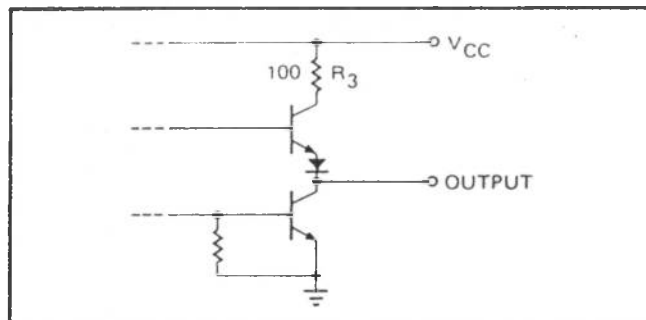


Figure 2. Output Schematic

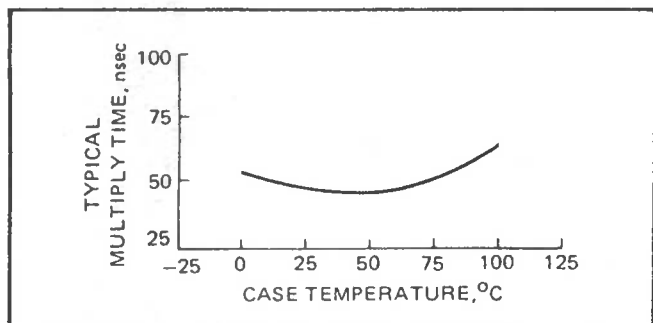


Figure 3. Multiply Time Versus Temperature

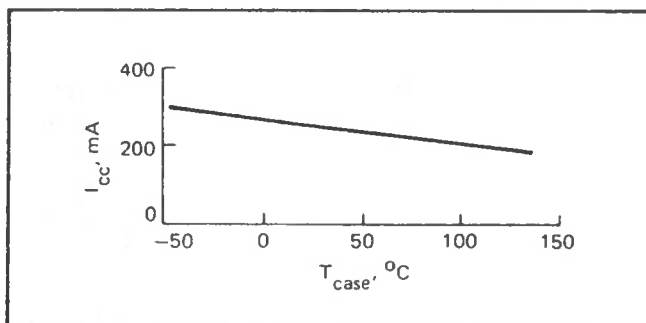


Figure 4. Typical I_{CC} Versus T_{case}

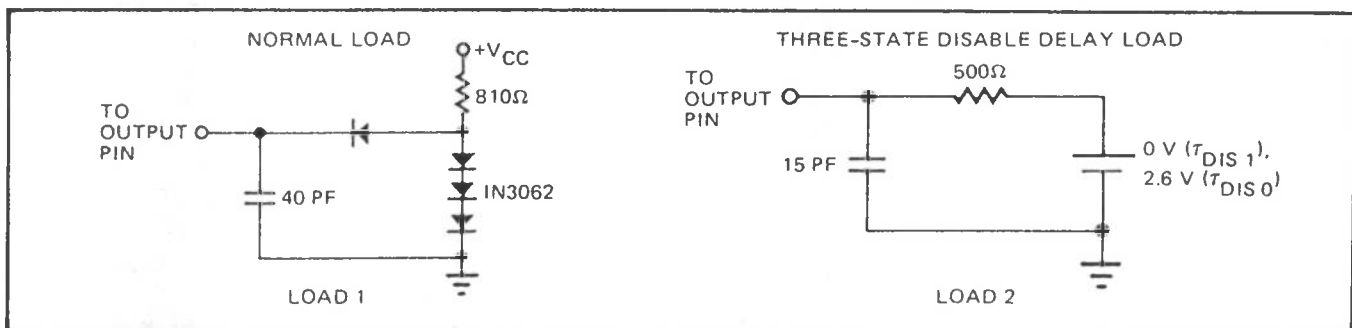


Figure 5. Test Loads for Delay Measurements

SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage	-0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range (T _{case})	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

Recommended operating conditions (required for the part to meet published specifications)

	MPY-8HUU MPY-8HUU-1			UNIT
	MIN	TYP*	MAX	
Supply voltage, V _{CC}	4.75	5.0	5.25	V
High-level output current, I _{OH}			-0.4	mA
Clock pulse width, t _{pw} (measured at 1.5 V level)	25			nsec
Input register setup time, t _S (see Figure 6)	25			nsec
Input register hold time, t _H (see Figure 6)	0			nsec
Operating temperature (T _{ambient})	0		70	°C

MPY-8HUI

SPECIFICATIONS

Electrical characteristics over recommended operating temperature ranges

PARAMETER		TEST CONDITIONS	MPY-8HUI MPY-8HUI-1			UNITS
			MIN	TYP*	MAX	
I_{IL} - Low level input current	RND, X_{in} , Y_{in}	$V_{CC} = \text{MAX}$ $V_{IL} = 0.4\text{V}$		- 200		μA
	CLKX, CLKY, TRIM, TRIL			- 0.5		mA
	CLKP			- 1.0		mA
I_{IH} - High level input current	RND, X_{in} , Y_{in}	$V_{CC} = \text{MAX}$ $V_{IL} = 2.4\text{V}$		25		μA
	CLKX, CLKY, TRIM, TRIL			25		μA
	CLKP			50		μA
V_{IL} - Low level input voltage						μA
V_{IH} - High level input voltage					0.8	V
V_{OL} - Low level output voltage		$V_{CC} = \text{MIN}$ $I_{OL} = 4.0\text{ mA}$ TRIM=TRIL=0 V	2.0			V
V_{OH} - High level output voltage		$V_{CC} = \text{MIN}$ $I_{OH} = -0.4\text{ mA}$ TRIM = TRIL = 0 V		0.3	0.5	V
I_{OH} HIZ - High impedance output current		$V_{CC} = \text{MAX}$ $V_{OH} = 2.4\text{ V}$ TRIM=TRIL=5.0 V	2.4	3.1		V
I_{OL} HIZ - High impedance output current		$V_{CC} = \text{MAX}$ $V_{OL} = 0.4\text{ V}$ TRIM=TRIL=5.0 V		25		μA
I_{CC} - Supply current		$V_{CC} = 5.25\text{ V}$ $T_A = 0^\circ\text{C}$				
		$V_{CC} = 5.0\text{ V}$ $T_A = 25^\circ\text{C}$		240		mA
		$V_{CC} = 5.25\text{ V}$ $T_A = 70^\circ\text{C}$				

Switching characteristics over the recommended temperature and voltage ranges

PARAMETER	CONDITIONS	TYP*	MPY-8HUI-1		MPY-8HUI		UNIT
			MIN	MAX	MIN	MAX	
T_{mc} Multiply time	See figure 6	45	10	65	10		nsec
T_o Output delay	Load 1 See figures 5, 6	25					nsec
T_{ENA} 3-state enable time	Load 1 See figures 5,6	25					nsec
T_{DIS} 3-state disable time	Load 2 See figures 5,6	20					nsec

*NOTE: At $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$

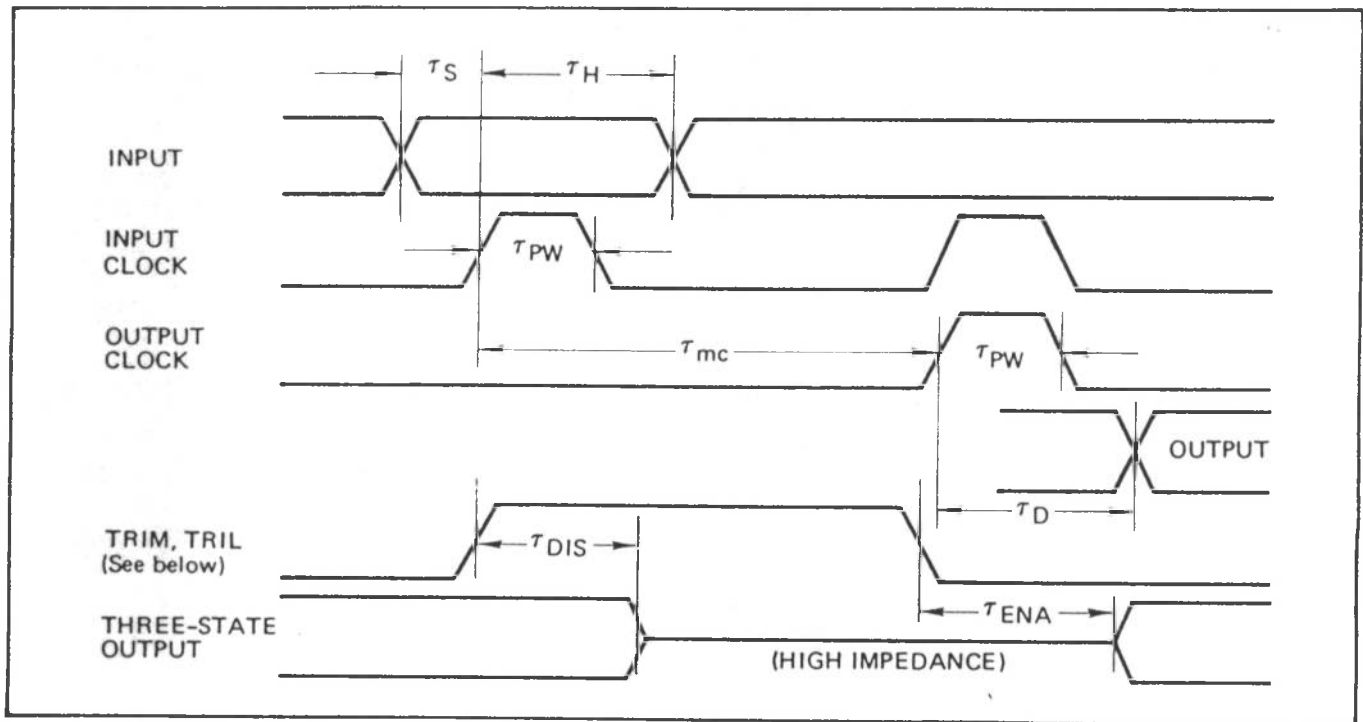


Figure 6. Timing Diagram

GLOSSARY OF TERMS

Commercial temperature range – 0 to 70°C still ambient air, case temperature stabilized under power.

Timing transitions – except for τ_{DIS} , all time measurements are made when a signal crosses 1.5V.

τ_{DIS1} – delay time from a 0 → 1 transition of TRIM or TRIL (measured at 1.5V), until the output pin under test drops 500mV below the previous quiescent logic 1 output voltage (See Figure below).

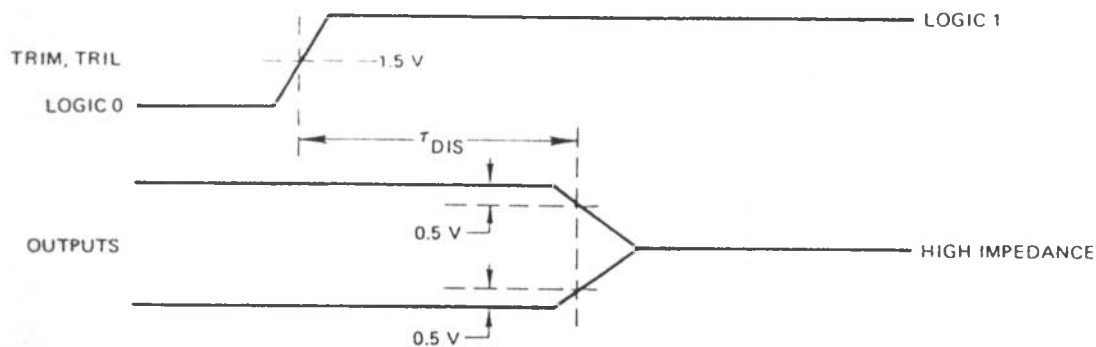
τ_{DIS0} – delay time from a 0 → 1 transition of TRIM or TRIL (measured at 1.5V), until the output pin under test rises 500mV above the previous quiescent logic 0 output voltage (See Figure below).

X_{in} , Y_{in} – Registered data input ports. X_7 and Y_7 are the MSB, X_0 and Y_0 are the LSB. Data is loaded into the X or Y input registers at the rising edge of CLK X or CLK Y, respectively.

RND – Registered control input, loaded on the rising edge of CLK X. Logic 1 – adds a one to the MSB bit of the LSP output word (P_7), rounding it into the MSP.

TRIM, TRIL – Logic 0 – The output 3-state buffers are enabled to become low impedance outputs.

Logic 1 – The output 3-state buffers are disabled to become high impedance outputs.



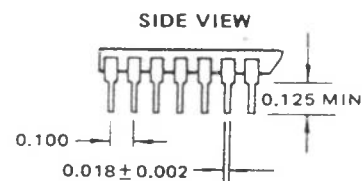
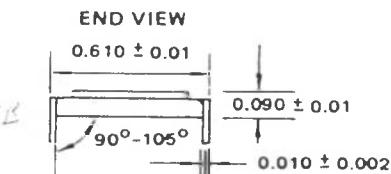
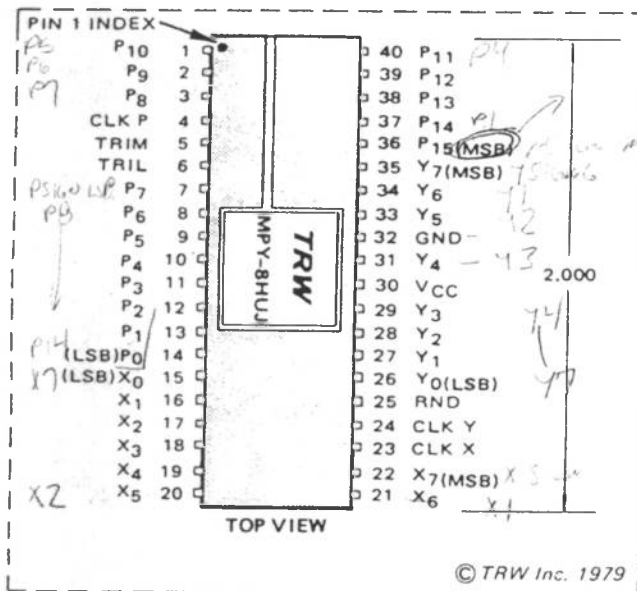
INPUT/OUTPUT FORMAT FOR INTEGER ARITHMETIC

X _{IN}								Y _{IN}							
X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
MSP								LSP							

INPUT/OUTPUT FORMAT FOR FRACTIONAL ARITHMETIC

X _{IN}								Y _{IN}							
X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶
P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
MSP								LSP							

PACKAGE INFORMATION



THERMAL RESISTANCE DATA

Case to ambient θ_{CA} (Still air) $\approx 25^\circ \text{C/W}$
Case to ambient θ_{CA} (300 cfm) $\approx 15^\circ \text{C/W}$

NOTE: DIMENSIONS IN INCHES

SOCKET INFORMATION

TYPE	40 PIN
Wire wrap	Excel 800B-003-40
Solder tail-tin plate	Cambion 703-4040-01-04-12
Solder tail-gold plate	Robinson Nugent ICN-406-S5-G
Zero insertion force	Textool 240-3346-00-0605

MPY-8HUJ

The MPY-8HUJ is an easy, low power way to upgrade the number-crunching capabilities of a microprocessor. Because the chip comes with input registers and output 3-states, the only other chips necessary are 4 SSI circuits to fully decode (if desired) the address and generate the interface control signals. Although the chip does have an output register, it can be made transparent to the microprocessor by continuously clocking it — no separate output clock instruction is required. In the application below, the three LSBs of the address bus plus the R/W line are decoded into control signals for the multiplier. Thus, only reads or writes to a small set of addresses are required in the software; the specific instructions are implicit in the addresses. The eight different addresses are given below.

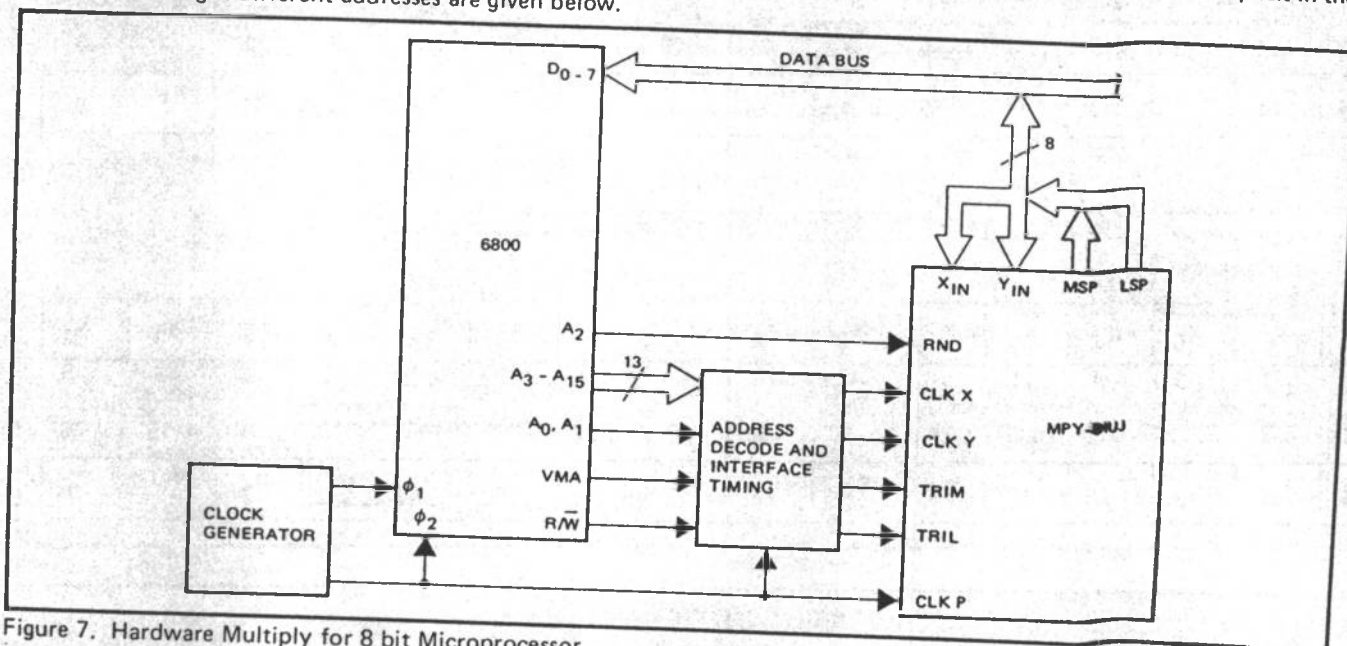


Figure 7. Hardware Multiply for 8 bit Microprocessor

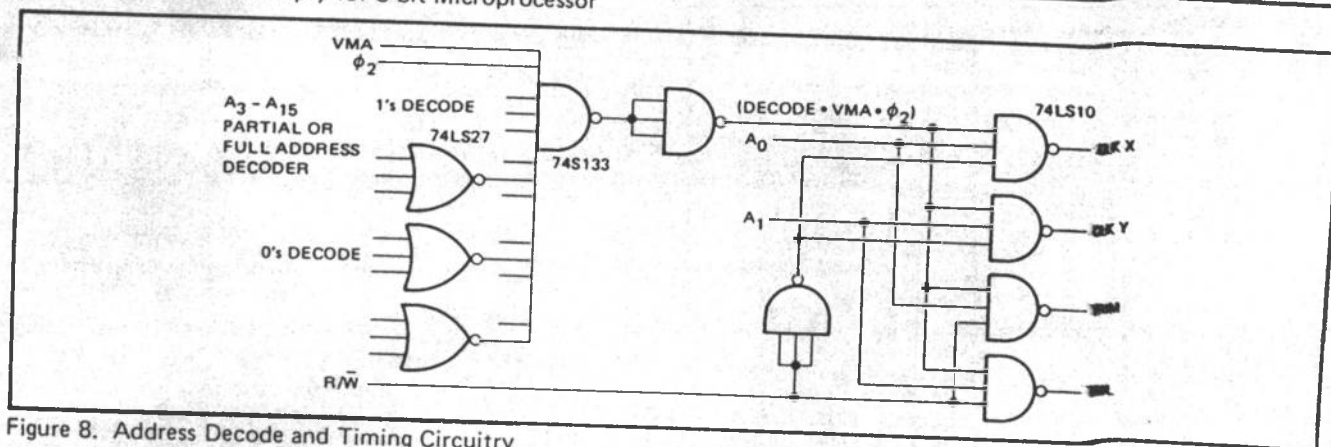


Figure 8. Address Decode and Timing Circuitry

MULTIPLIER INSTRUCTIONS

ADDRESS	WRITE	READ
XXX0	No-op load (interface test)	No-op read (open bus)
1	Load X register, RND = 0	Read most significant product (MSP)
2	Load Y register, RND = 0	Read least significant product (LSP)
3	Load X and Y simultaneous, RND = 0	Do not use! (two 3-bits on at once)
4	No-op load	Same as 0
5	Load X, RND = 1	Same as 1
6	Load Y, RND = 1	Same as 2
XXX7	Load X and Y simultaneous, RND = 1	Same as 3

TRW reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of TRW Inc. or others.

TRW SALES OFFICES

ALABAMA, Huntsville	(205) 533-7600	MISSOURI, St. Louis	(314) 432-2830
ARIZONA, Phoenix	(602) 971-6250	NEBRASKA, Lincoln	(402) 474-5151
CALIFORNIA, Los Angeles	(213) 478-0183	NEW MEXICO, Albuquerque	(505) 292-0428
San Diego	(714) 571-1544	NEW YORK, Rochester	(716) 424-2830
Mountain View	(415) 969-6060	NORTH CAROLINA, Charlotte	(704) 527-1344
Tustin	(714) 973-2162	OHIO, Cincinnati	(513) 521-2290
COLORADO, Westminster	(303) 426-0890	Columbus	(614) 888-9396
CONNECTICUT, Orange	(203) 795-3515	Dayton	(513) 298-9546
Rowayton	(203) 853-4466	Middleburg Heights	(216) 826-4424
FLORIDA, Ft. Lauderdale	(305) 772-3000	OREGON, Beaverton	(503) 643-1644
Orlando	(305) 857-3650	PENNSYLVANIA, Bala Cynwyd	(215) 667-3400
GEORGIA, Norcross	(404) 447-6154	Pittsburgh	(412) 344-7277
ILLINOIS, Elk Grove Village	(312) 593-0200	TENNESSEE, Greeneville	(615) 639-6154
INDIANA, Fort Wayne	(219) 432-5591	TEXAS, Austin	(512) 451-2959
Indianapolis	(317) 359-9283	Dallas	(214) 387-3030
Kokomo	(317) 457-9127	Houston	(713) 772-5541
IOWA, Cedar Rapids	(319) 393-8703	UTAH, Salt Lake City	(801) 486-5473
KANSAS, Prairie Village	(913) 236-4646	VIRGINIA, Richmond	(804) 288-8334
Wichita	(316) 686-6685	WASHINGTON, Bellevue	(206) 454-0300
KENTUCKY, Louisville	(502) 426-7696	WISCONSIN, Brookfield	(414) 475-7755
MARYLAND, Baltimore	(301) 426-1241	CANADA	
MASSACHUSETTS, Waltham	(617) 890-3232	BRITISH COLUMBIA,	
MICHIGAN, Grand Rapids	(616) 942-5420	Vancouver	(604) 874-2422
Southfield	(313) 559-5454	MANITOBA, Winnipeg	(204) 775-3354
St. Joseph	(616) 983-7337	ONTARIO, Toronto	(416) 494-5445
MINNESOTA, Minneapolis	(612) 854-4600	QUEBEC, Montreal	(514) 341-6428

INTERNATIONAL SALES OFFICES

ARGENTINA, Buenos Aires	30-4132	JAPAN, Tokyo	4615121
AUSTRALIA, Moorabbin, Vic.	951566	NETHERLANDS, Amsterdam	934824
AUSTRIA (see Germany)		NEW ZEALAND, Wellington	51279
BELGIUM, Brussels	6600012	NORWAY, Oslo	02-786210
BRAZIL, Sao Paulo	2409211	SOUTH AFRICA, Capetown	457656
DENMARK, Herlev	842000	Johannesburg	6181027
FINLAND, Helsinki	692-6022	SPAIN, Madrid	2425204
FRANCE, Paris	7581111	SWEDEN, Stockholm	08635040
GERMANY, Munich	7146065	SWITZERLAND, Zurich	429900
ISRAEL, Tel Aviv	444572	TAIWAN, Taipei	7512062-3
ITALY, Monza	360021	UNITED KINGDOM, London	9025941

TRW LSI PRODUCTS

2525 E. EL SEGUNDO BLVD., EL SEGUNDO, CA 90245
(213) 535-1831